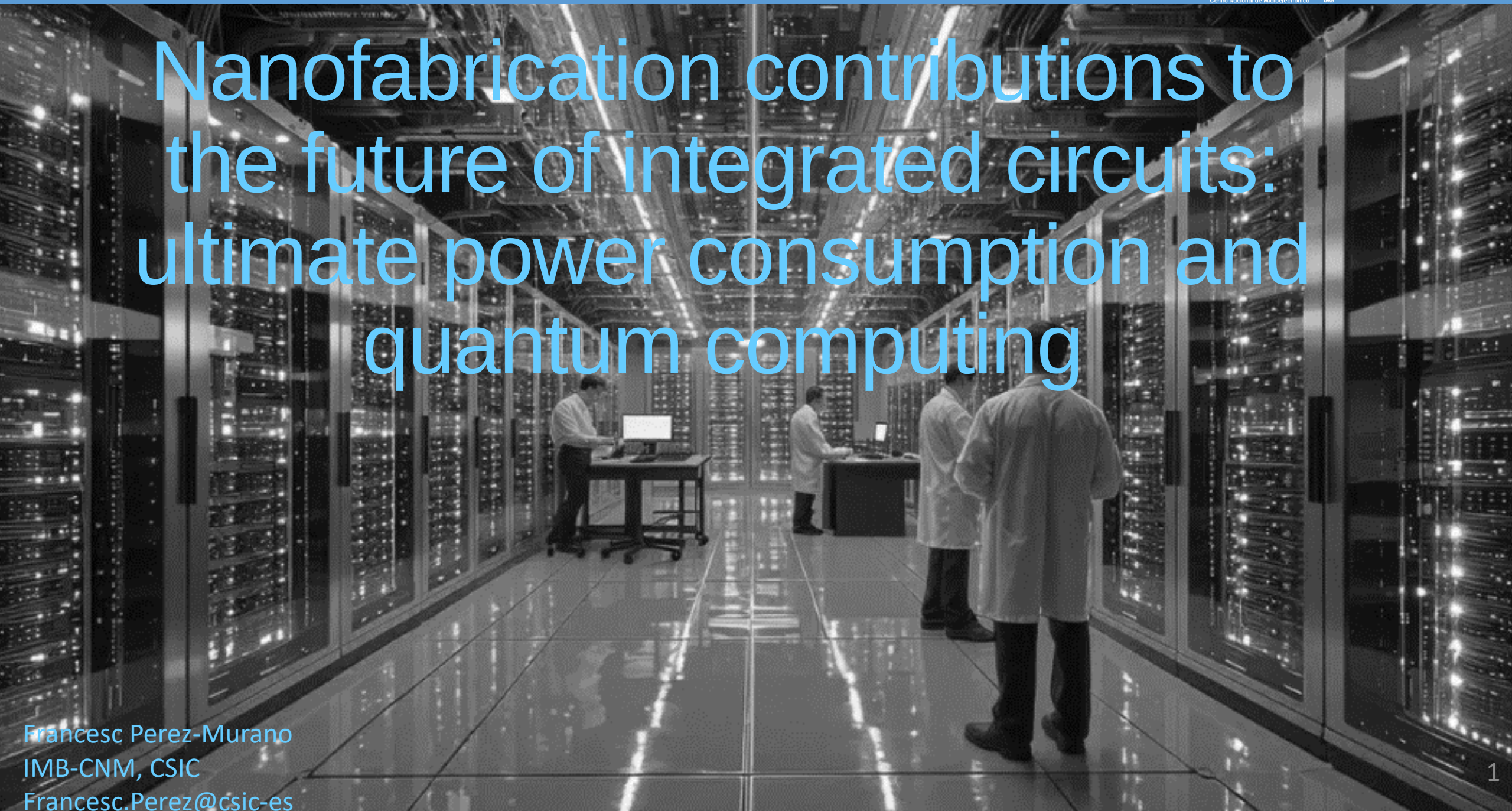


Nanofabrication contributions to the future of integrated circuits: ultimate power consumption and quantum computing

Francesc Perez-Murano
IMB-CNM, CSIC
Francesc.Perez@csic-es

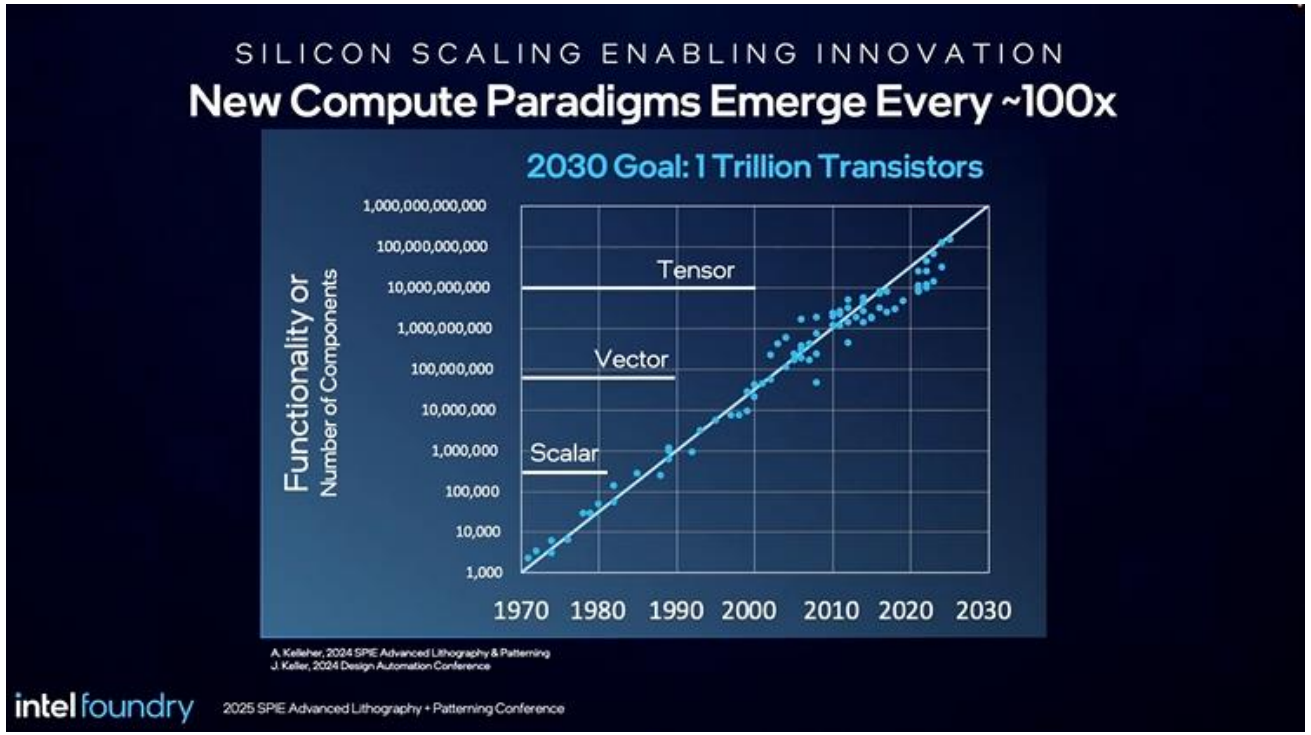
Shown at the SPIE Advanced Lithography and patterning conference. San Jose, CA. February 2025

Eric A. Karl "Evolutions in technology enabling the AI era", Proc. SPIE 13425, DTCO and Computational Patterning IV, 1342502 (23 April 2025); https://doi.org/10.1117/12.3056887

Has Moore's law era ended?

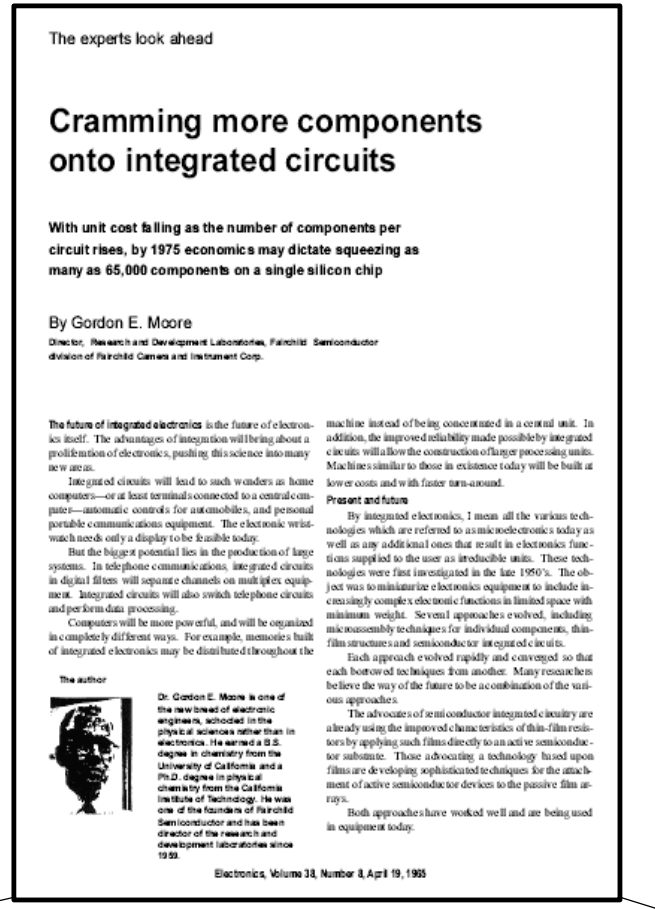
NO!!!!

Moore's law



Eric A. Karl "Evolutions in technology enabling the AI era", Proc. SPIE 13425, DTCO and Computational Patterning IV, 1342502 (23 April 2025); https://doi.org/10.1117/12.3056887

Electronics, April 19, 1965



The experts look ahead

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

Computers will be more powerful, and will be organized in completely different ways. For example, memories built of integrated electronics may be distributed throughout the machine instead of being concentrated in a central unit. In addition, the improved reliability made possible by integrated circuits will allow the construction of larger processing units. Machines similar to those in existence today will be built at lower costs and with faster turn-around.

Present and future

By integrated electronics, I mean all the various technologies which are referred to as microelectronics today as well as any additional ones that result in electronics functions supplied to the user as irreducible units. These technologies were first investigated in the late 1950's. The object was to miniaturize electronics equipment to include increasingly complex electronic functions in limited space with minimum weight. Several approaches evolved, including microassembly techniques for individual components, thin-film structures and semiconductor integrated circuits.

Each approach evolved rapidly and converged so that each borrowed techniques from another. Many researchers believe the way of the future to be a combination of the various approaches.

The advocates of semiconductor integrated circuitry are already using the improved characteristics of thin-film resistors by applying such films directly to an active semiconductor substrate. Those advocating a technology based upon films are developing sophisticated techniques for the attachment of active semiconductor devices to the passive film arrays.

Both approaches have worked well and are being used in equipment today.

The author

Dr. Gordon E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been director of the research and development laboratories since 1959.

Electronics, Volume 38, Number 8, April 19, 1965

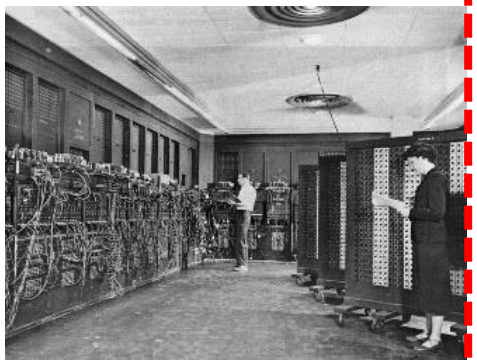
Miniaturization in microelectronics **for more than six decades** has enabled **increased performance** of integrated circuits (ICs) with **reduced power consumption** per device.

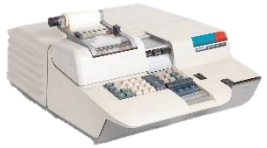
which must be driven is distinctly limited. In fact, shrinking dimensions on an integrated structure makes it possible to operate the structure at higher speed for the same power per unit area.

Vaccuum electronics

Microelectronics

Nanoelectronics





1940 | 1960 | 1980 | 2000 | 2020

Válvula termoiónica

Transistor de Si

1 transistor

TTL Quad Gate

16 transistors

8-bit Micropro

4500 transistors

32-bit Micropro

275 k transistors

32-bit Micropro

3 100 k transistors

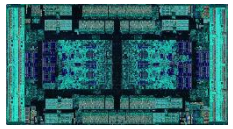
64-bit Micropro

562 M transistors

3072-Core GPU

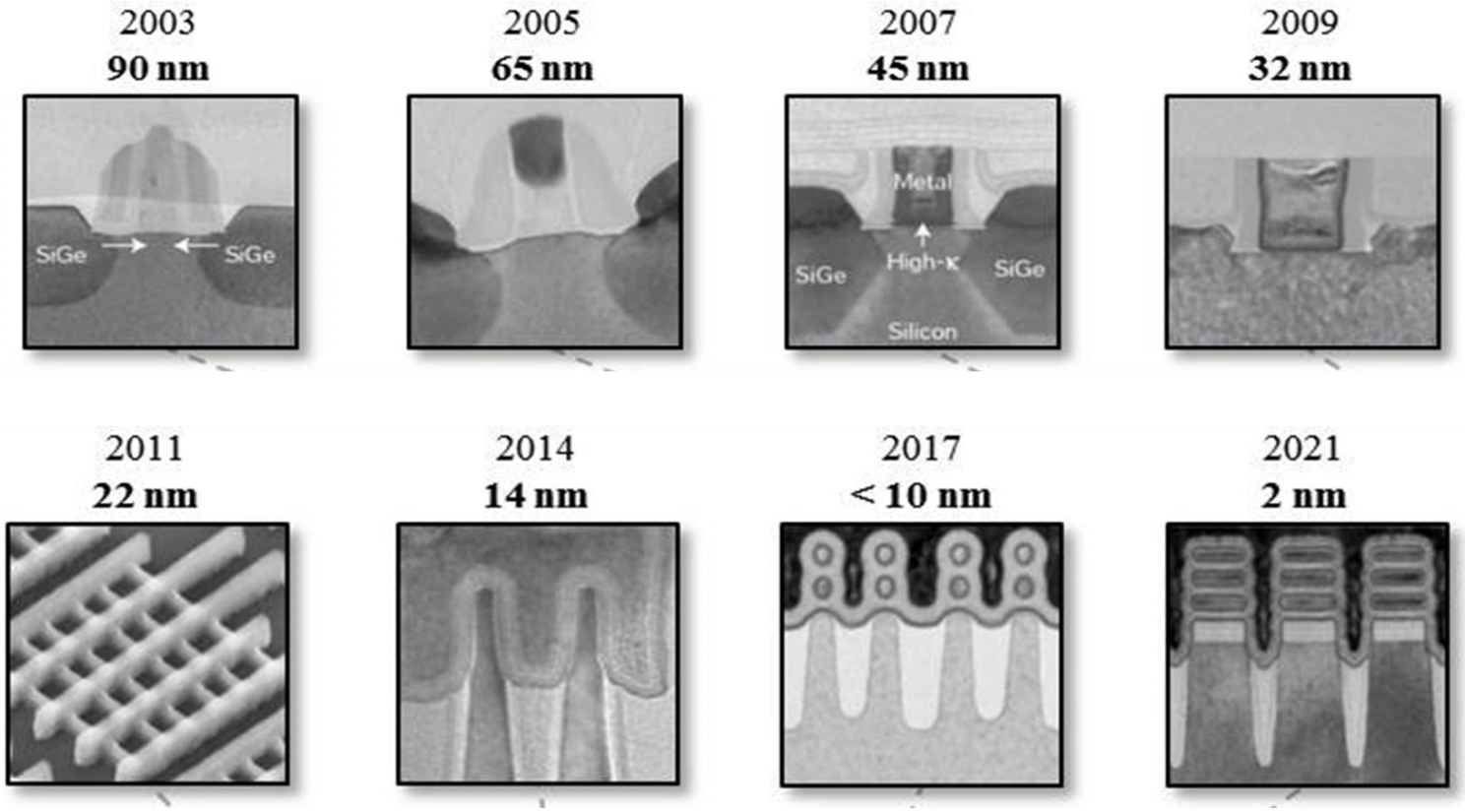
8 G transistors

AMD Epyc Rome



40 G transistors

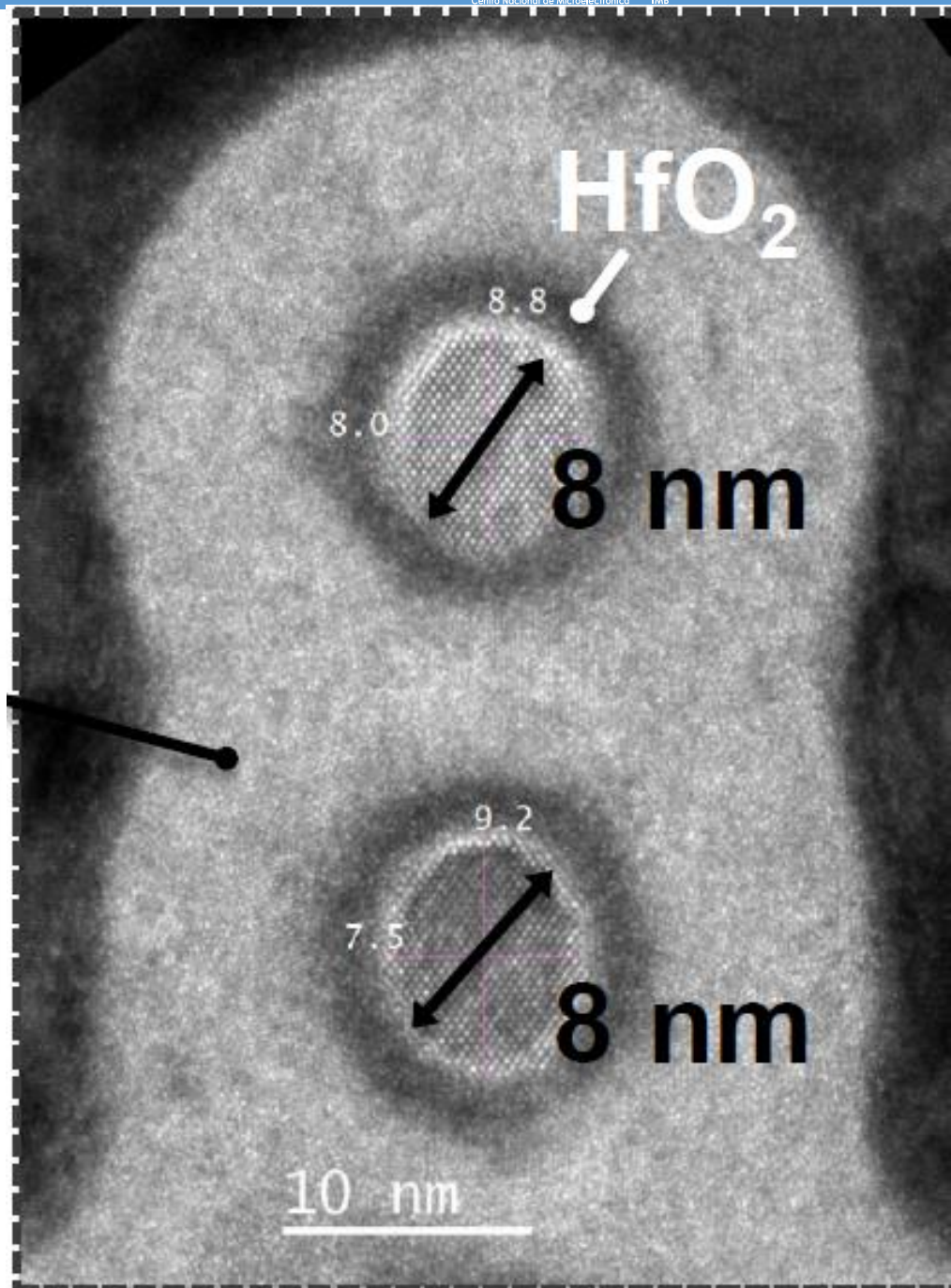
Integrated circuit technology



Alberto del Moral. PhD Thesis

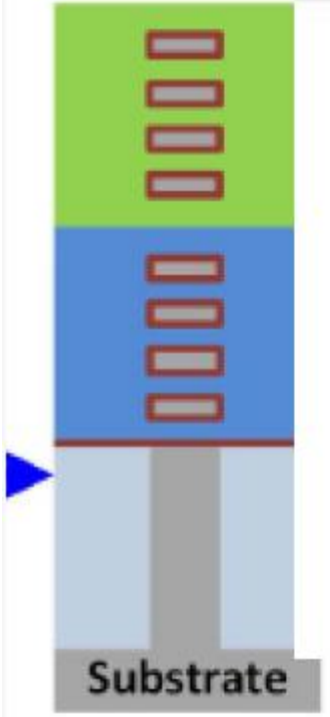
Current density integration: 10^9 transistors per mm^2

Hans Mertens. Imec. SemiconEuropa, TechArena, Advanced Materials Session, 15/11/2017



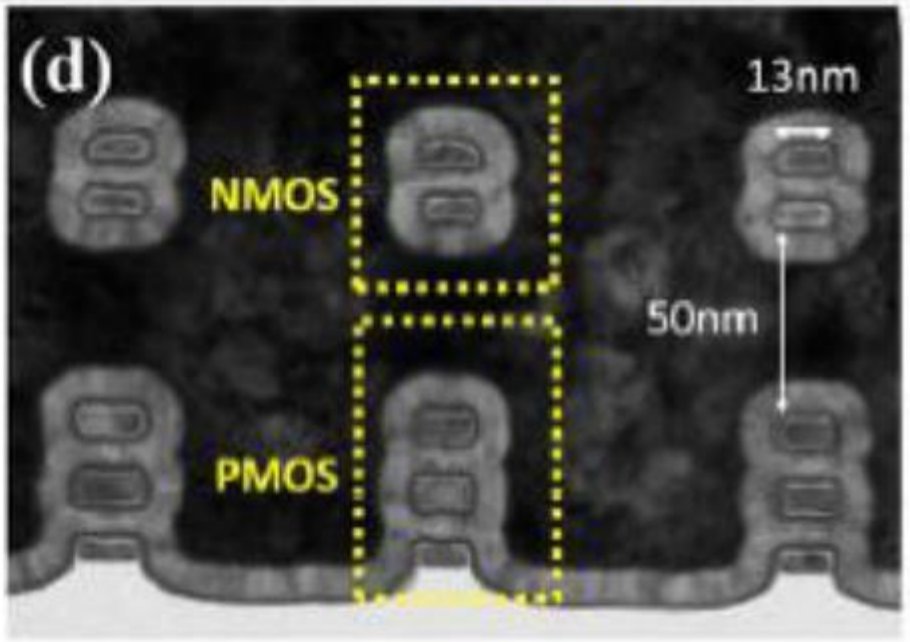
Presently, the level of dimensional control and material composition is approaching the single atom accuracy.

Stacked CMOS



3-D Self-aligned Stacked NMOS-on-PMOS Nanoribbon Transistors for Continued Moore's Law Scaling

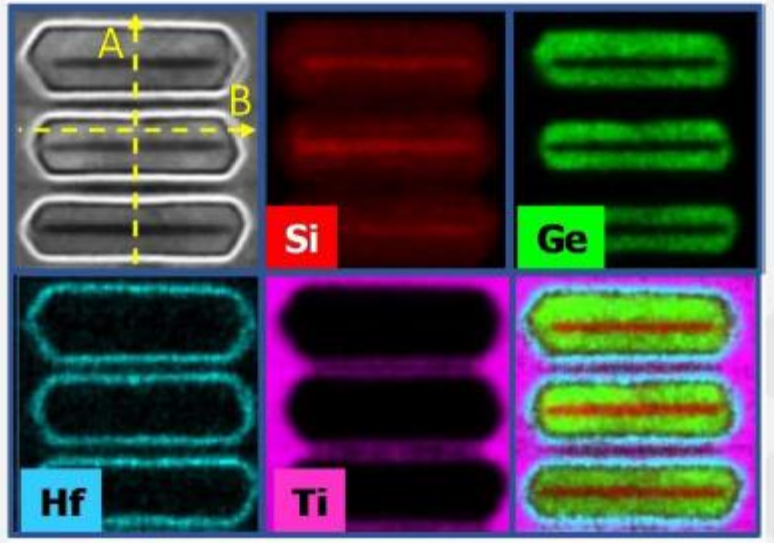
C.-Y. Huang[1], G. Dewey[1], E. Mannebach[1], A. Phan[1], P. Morrow[1], W. Rachmady[1], I.-C. Tung[1], N. Thomas[1], U. Alaan[2], R. Paul[1], N. Kabir[1], B. Krist[1], A. Oni[2], M. Mehta[2], M. Harper[2], P. Nguyen[2], R. Keech[2], S. Vishwanath[2], K. L. Cheong[2], J. S. Kang[2], A. Lilak[2], M. Metz[1], S. Clendenning[1], B. Turkot[1], R. Schenker[1], H. J. Yoo[1], M. Radosavljevic[1], and J. Kavalieros[1]
[1]Components Research, [2]Technology Development, Intel Corporation, Hillsboro, OR 97124, USA
email: cheng-ying.huang@intel.com

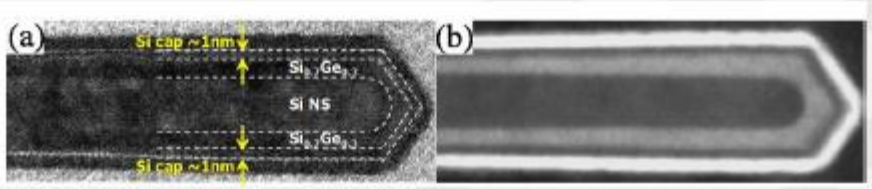


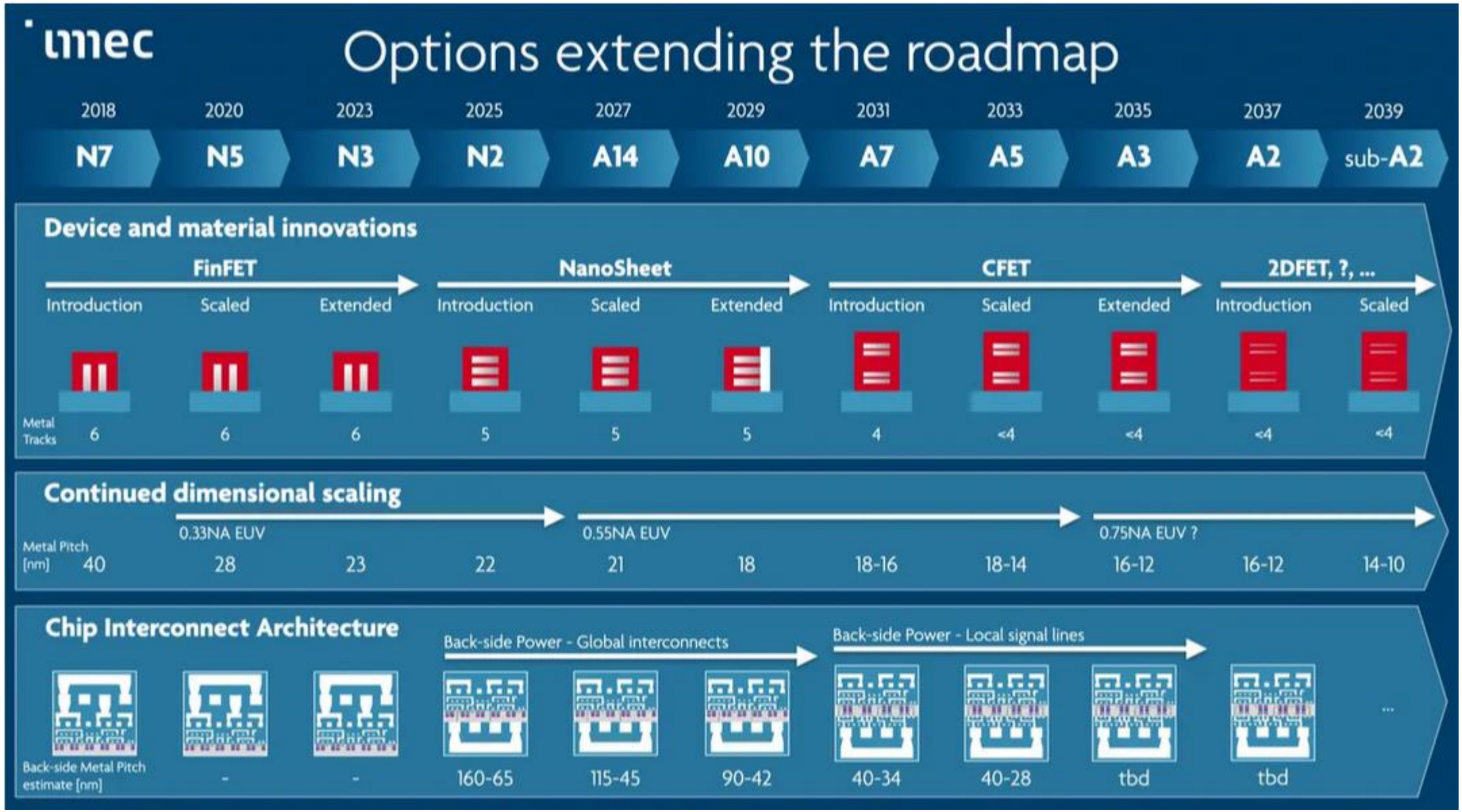
IEDM 2020

Stacked Gate-All-Around Nanosheet pFET with Highly Compressive Strained $Si_{1-x}Ge_x$ Channel

S. Mochizuki, M. Bhuiyan, H. Zhou, J. Zhang, E. Stuckert, J. Li, K. Zhao, M. Wang, V. Basker, N. Loubet, D. Guo, B. Haran, and H. Bu
IBM Research, 257 Fuller Road, Suite 3100, Albany, NY 12203, email: smochiz@us.ibm.com

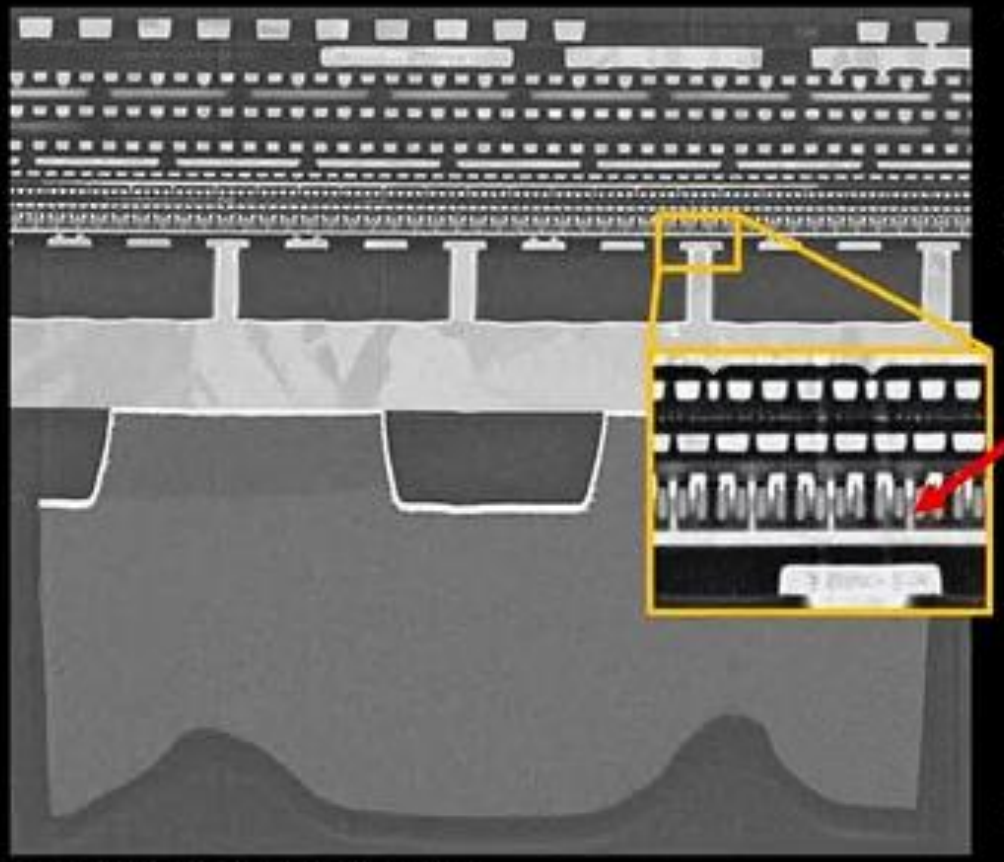






Christophe Fouquet. ASML. **Scaling to support Moore's Law through the AI era**. SPIE Advanced Lithography and Patterning. San Jose, CA. 2025

State-of-the-art Nanosheet-based Logic Technology



- **BEOL process and materials** improve R*C delay and enable logic density gain
- **Nanosheet devices** offer excellent power efficiency from structural and DTCO innovations
- **Backside contact** preserves gate density and device width flexibility
- **Backside metallization** improves power delivery, chip density and performance

Source: TSMC 2024 Technology Symposium

Source: 2024 IEDM Plenary

Michael Wu. TSMC. Riding the wave of AI with semiconductor technology innovations. SPIE Advanced Lithography and Patterning. San Jose. 2025

New players: 3D Integration

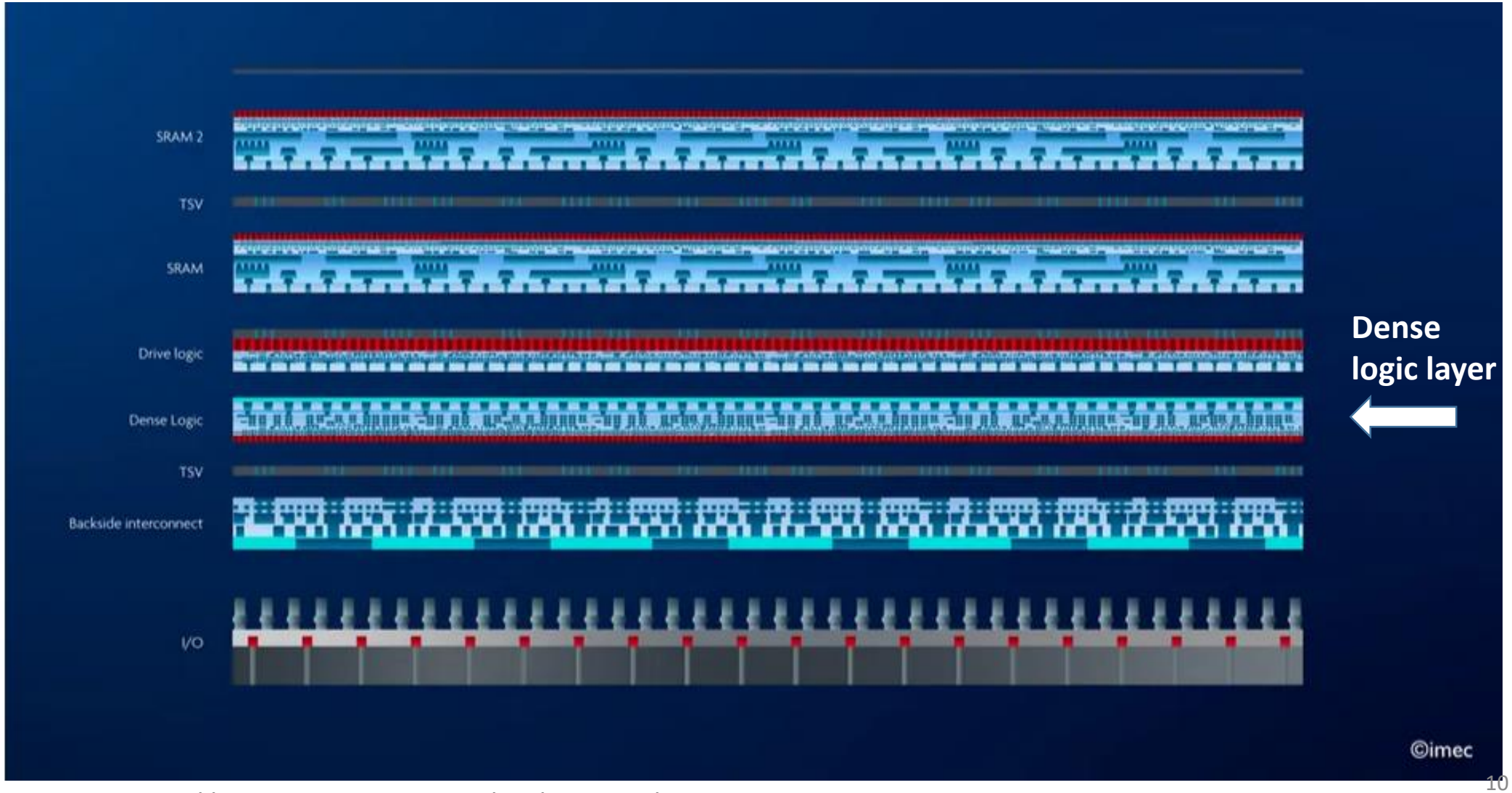
CMOS 2.0

Wafer to wafer bonding

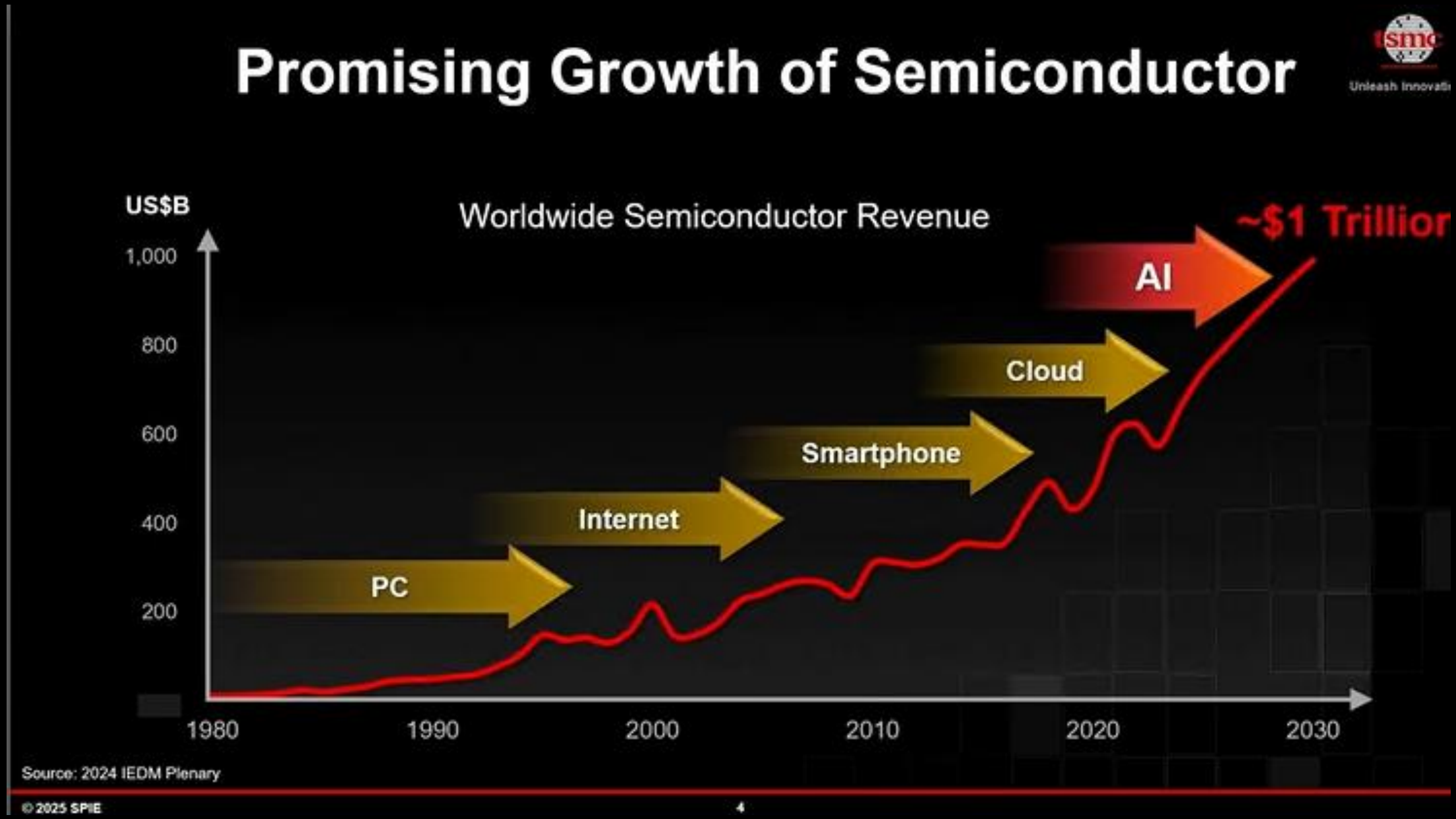
Backside power delivery network (BSPDN)

System on Chip (SoC)

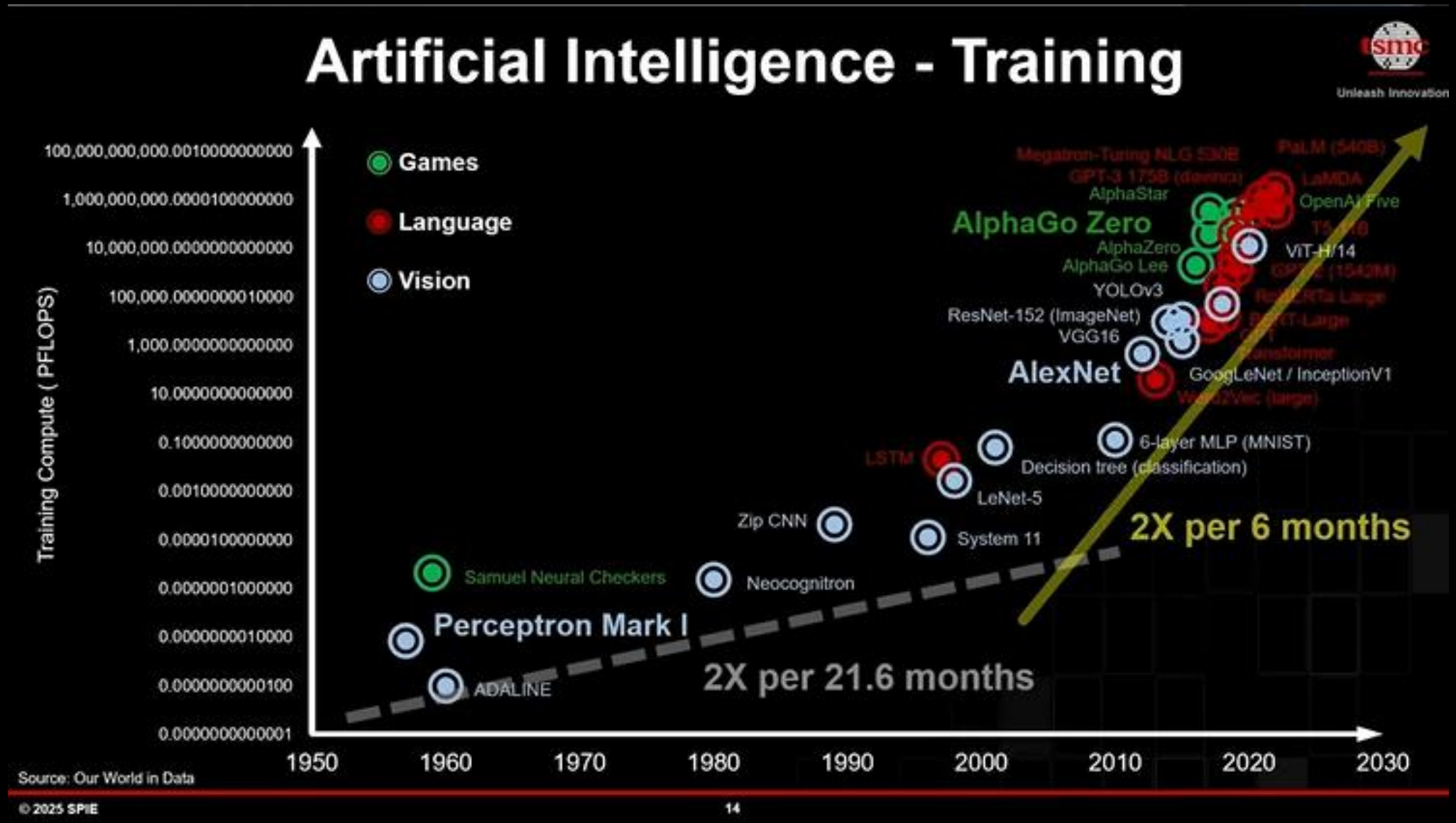
Design-technology co-optimization (DTCO)



https://www.imec-int.com/en/articles/cmos-20-bringing-heterogeneity-inside-system-chip

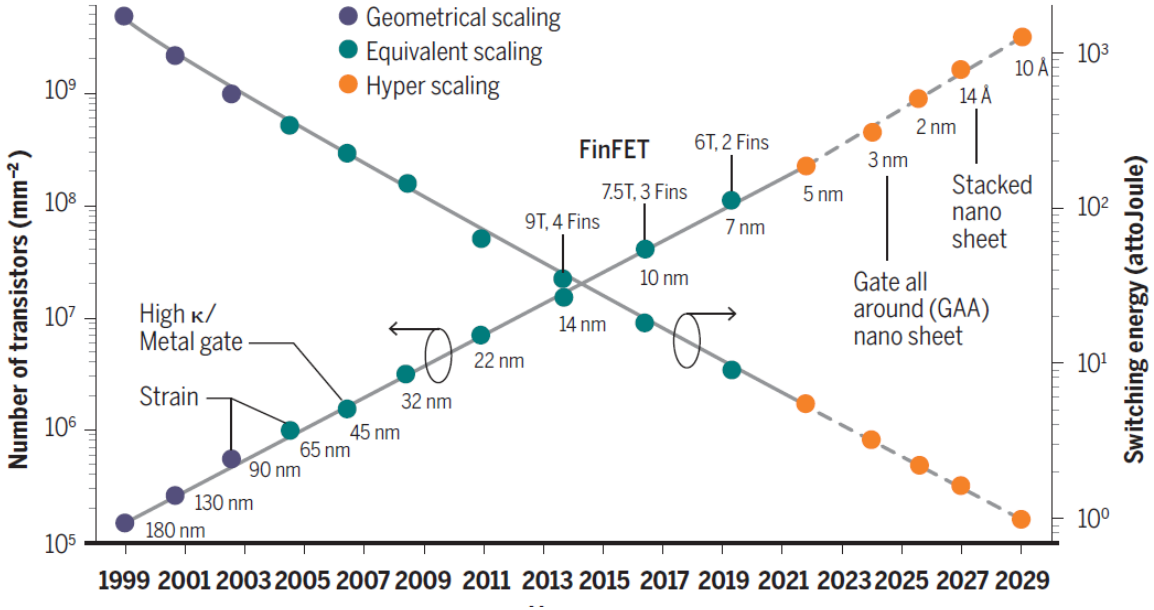


Michael Wu. TSMC. Riding the wave of AI with semiconductor technology innovations. SPIE Advanced Lithography and Patterning. San Jose. 2025

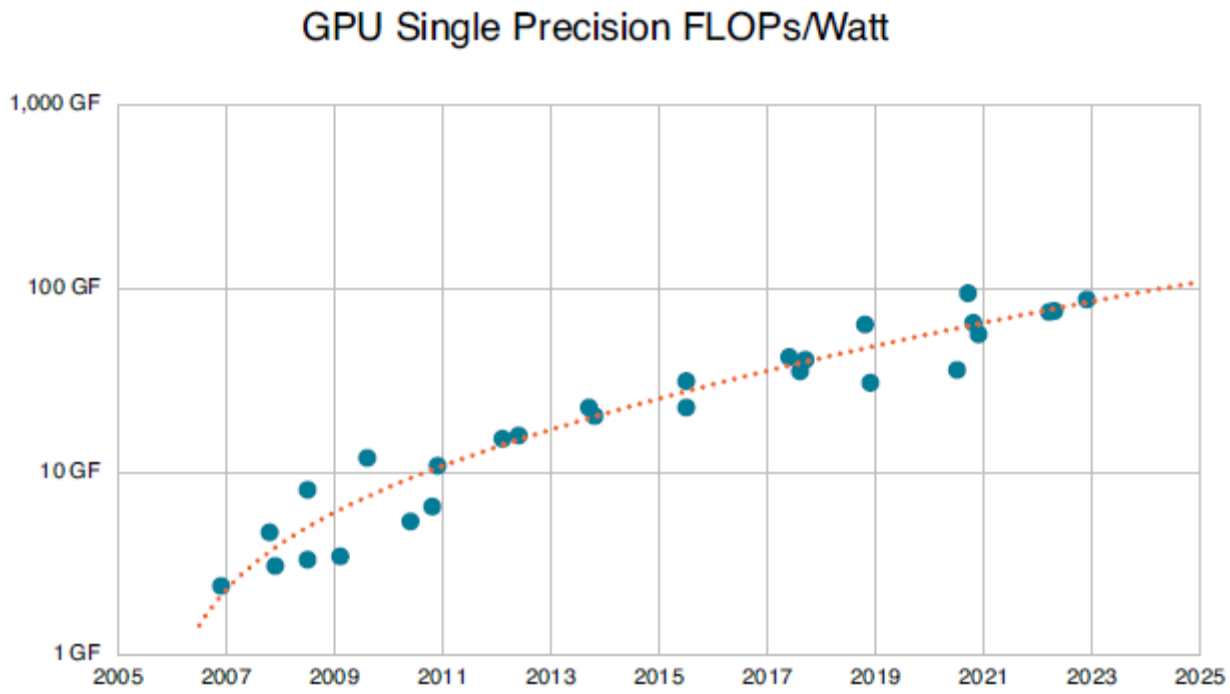


Michael Wu. TSMC. Riding the wave of AI with semiconductor technology innovations. SPIE Advanced Lithography and Patterning. San Jose. 2025

Energy consumption per operation



Datta, Suman, Wriddhi Chakraborty, and Marko Radosavljevic.
"Toward attojoule switching energy in logic transistors."
Science 378.6621 (2022): 733-740.

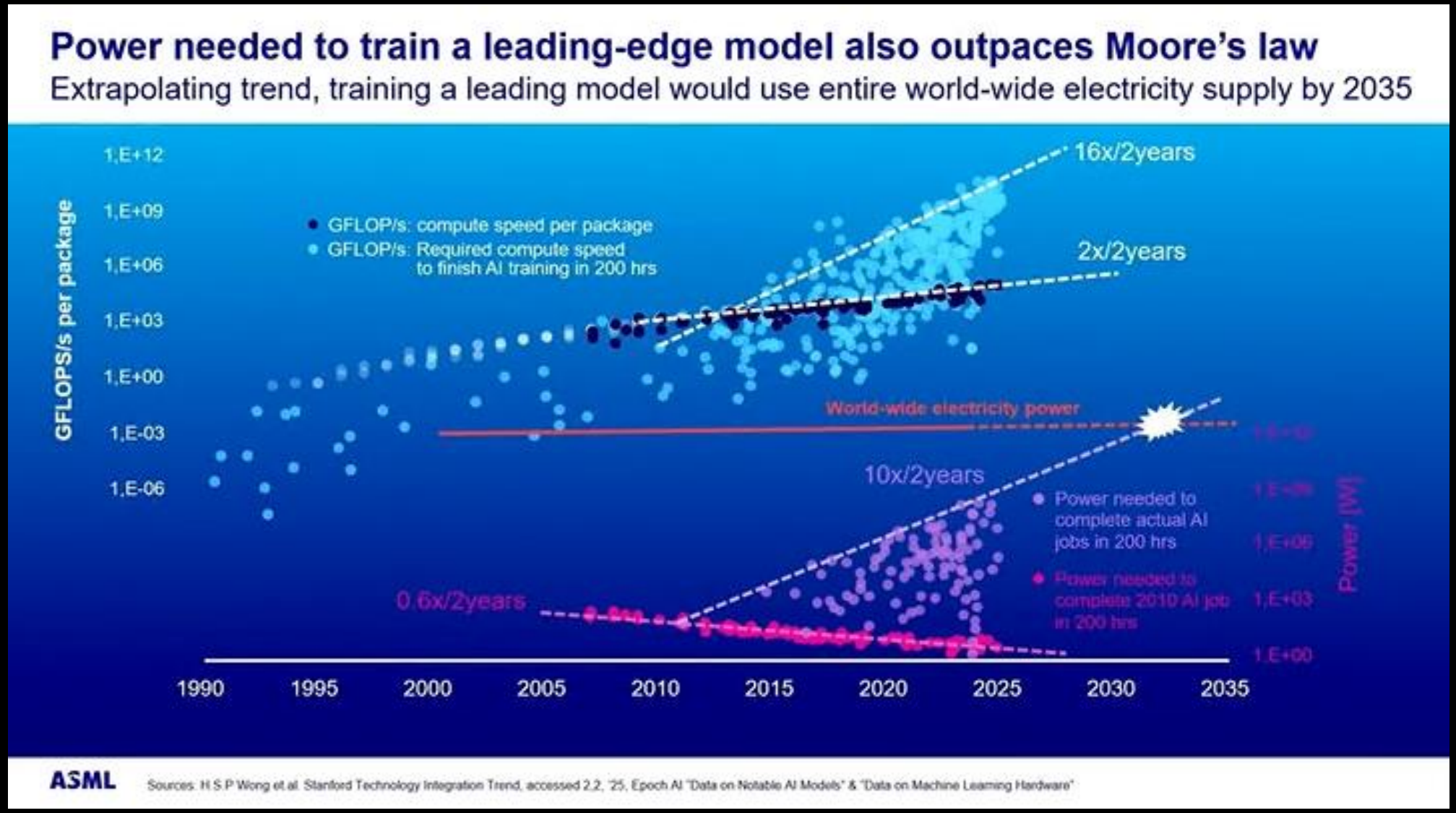


Su, Lisa, and Sam Naffziger.
" Innovation For the Next Decade of Compute Efficiency."
2023 IEEE International Solid-State Circuits Conference (ISSCC). IEEE, 2023.

100 GFLOPs/s Watt

10^9 GFLOPs/s -> 10 MW

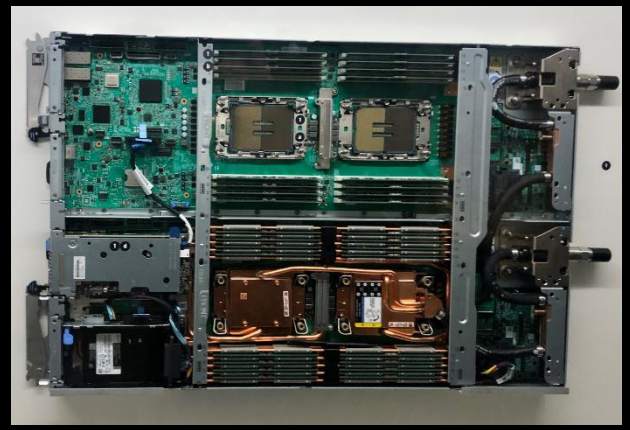
10^{12} GFLOPs/s -> 10 GW

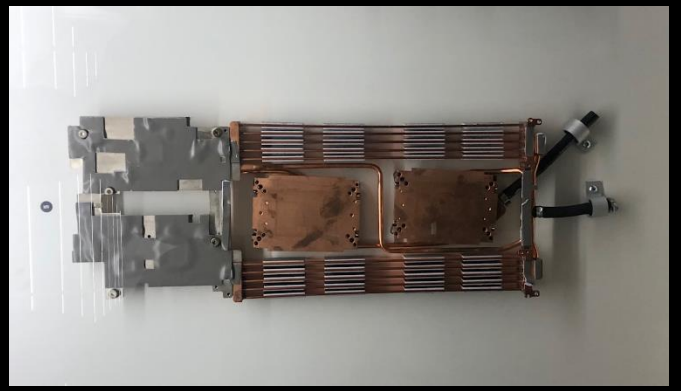


Electrical power today needed for a data center: 100 MW
Electrical power needed in 2033: 1 TW

Maximum electrical power available in **Catalonia** in 2023: 12GW
Maximum electrical power available in **Catalonia from renovable sourcers** in 2023 : 4 GW
Maximum electrical power available in **Spain from nuclear energy:** 7.4 GW

Visit to a Supercomputer: Mare Nostrum 5. April 2, 2025





SUPERCOMPUTING CENTERS: Power consumption

Fastest

#18 El Capitan. LLNL, USA.

1.724 Pflop/s. **(#1 in speed)**

Power: 29.6 MW

59 Gflops/Watt

11.039.616 Cores AMD

2nd fastest

#22 Frontier. Oak Ridge, USA.

1.353 Pflop/s **(#2 in speed)**

Power: 24.6 MW

55 Gflops/watt

9.066.176 Cores AMD.

More efficient

#1 JEDI-JUPITER. Jülich.

4.5 Pflop/s (#222 in speed)

Power: 67 kW

72 Gflops/watt

19.584 Cores NVIDIA

Mare Nostrum at BSC

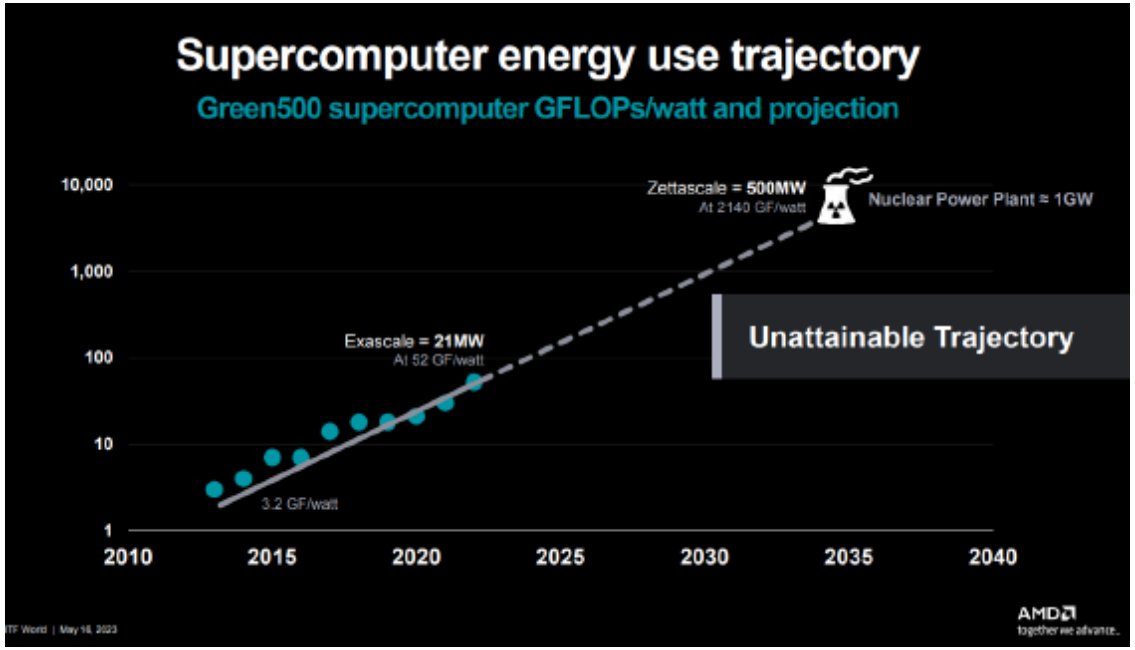
#31 Mare Nostrum 5, Barcelona

175 Pflop/s (#11 en velocitat)

Power: 4.2 MW

48 Gflops/watt

663.040 Cores NVIDIA.



https://www.top500.org/lists/green500/2024/11/

NANOFABRICATION CONTRIBUTONS FOR FUTURE IC PROCESSING at IMB-CNM

The flagship center in Spain dedicated to micro and nano electronics

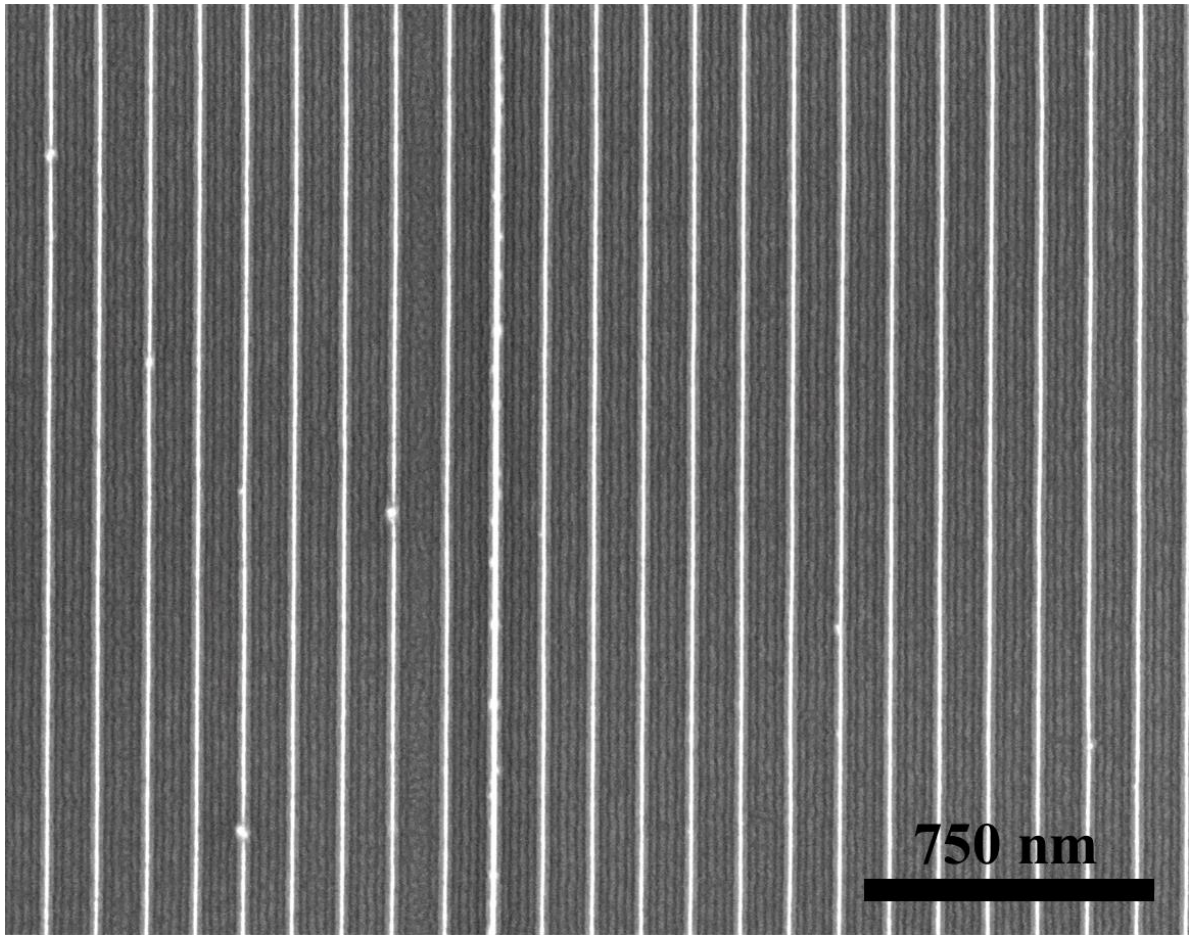
Micro/Nano fabrication clean room

www.imb-cnm.csic.es

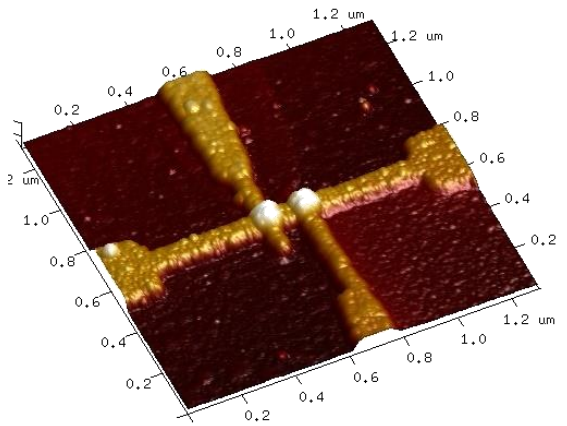
To push the limits of current technology , research is needed

Pushing down lithography resolution

Directed self assembly of block co-polymers

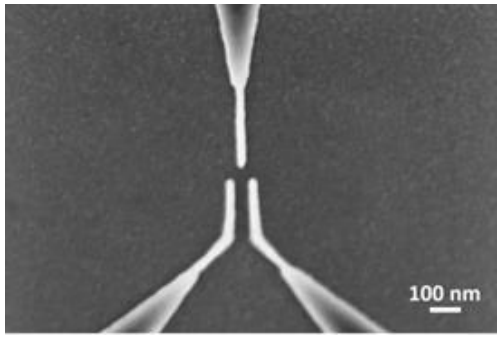


Beyond CMOS devices



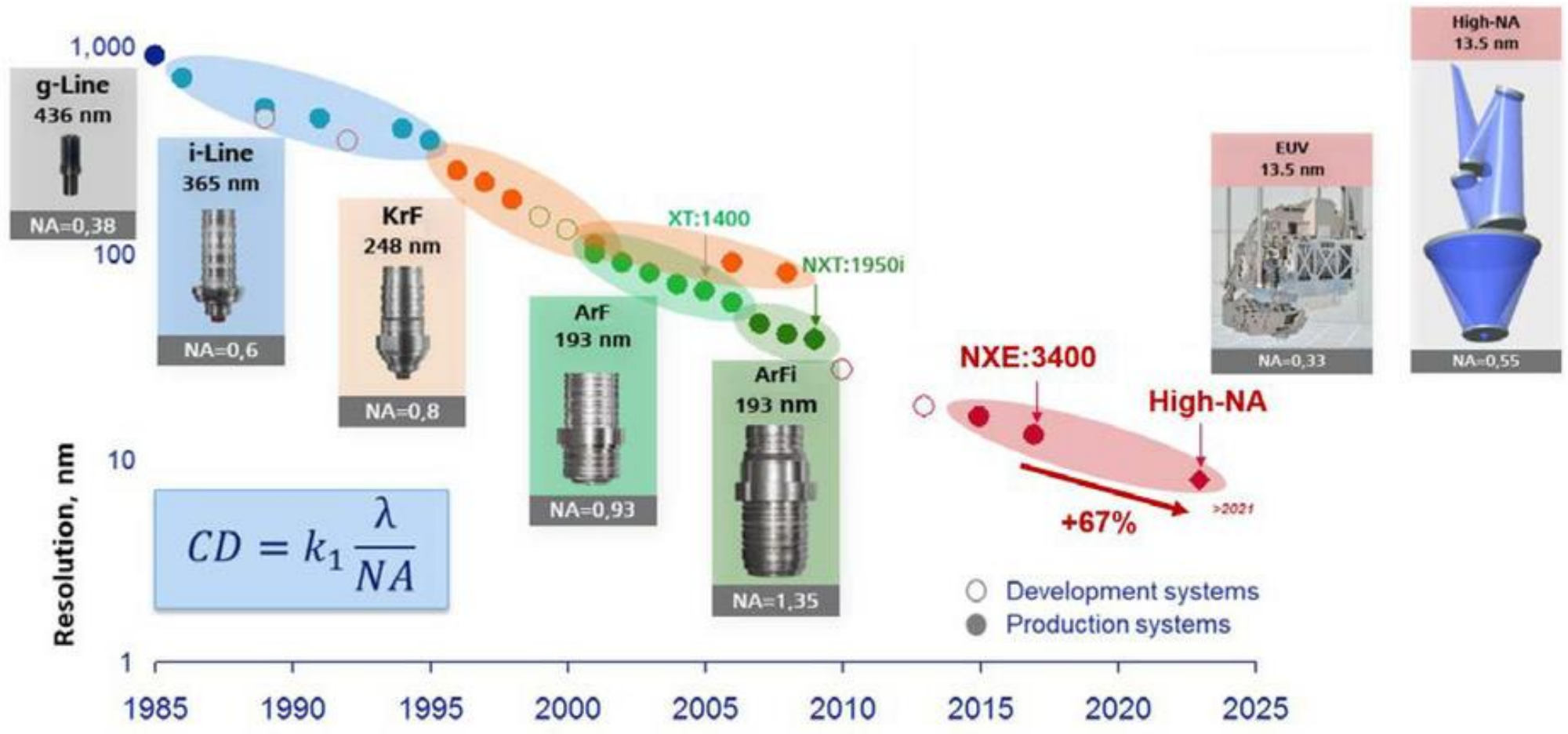
Single electron devices

Quantum computing

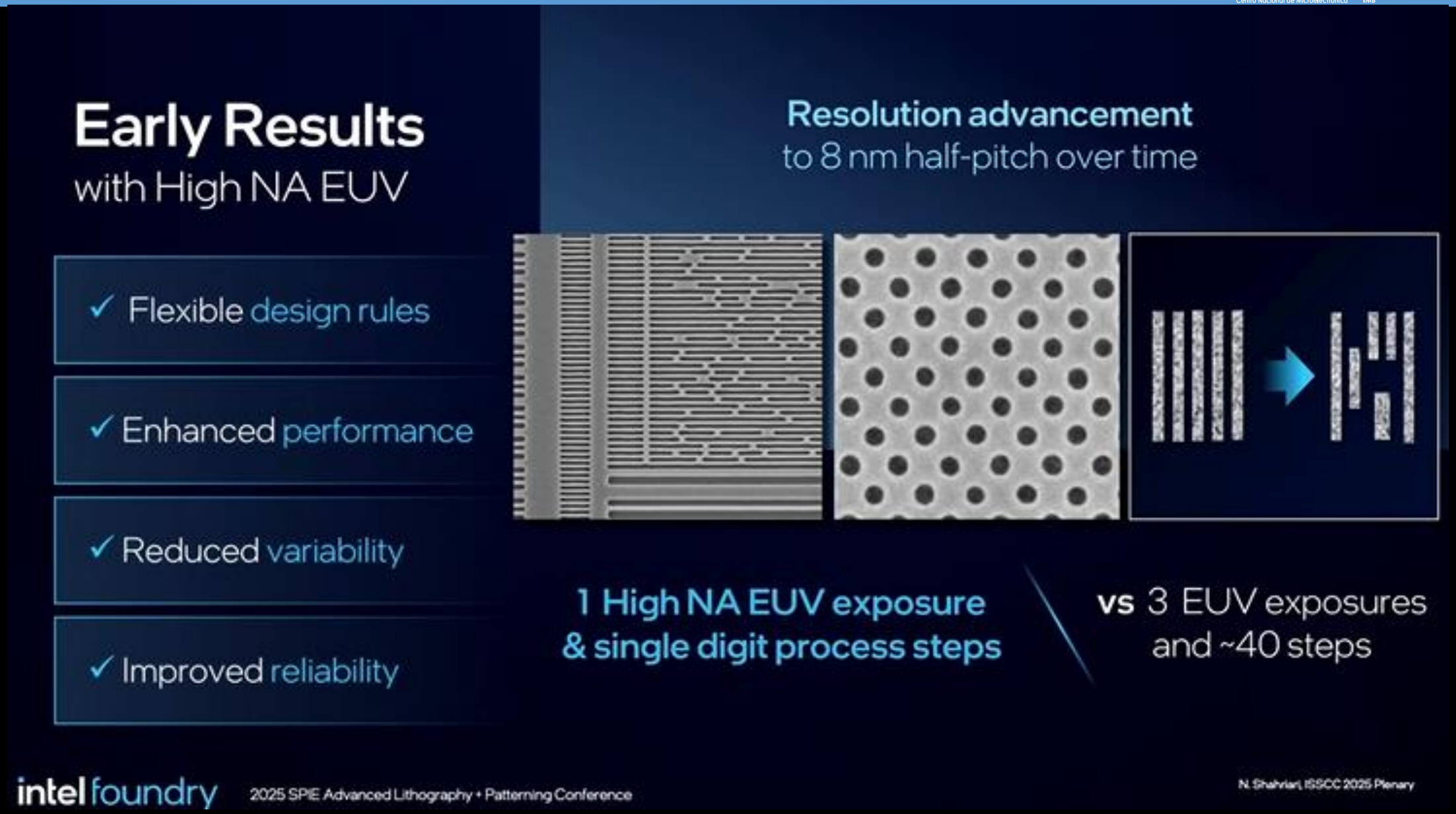


Platform for semiconductor spin qubit fabrication

Directed self assembly of block co-polymers



"EUV optics: status, outlook and future", Paul Graeupner et al, Proceedings Volume 12051, Optical and EUV Nanolithography XXXV; 1205102 (2022)
https://doi.org/10.1117/12.2614778

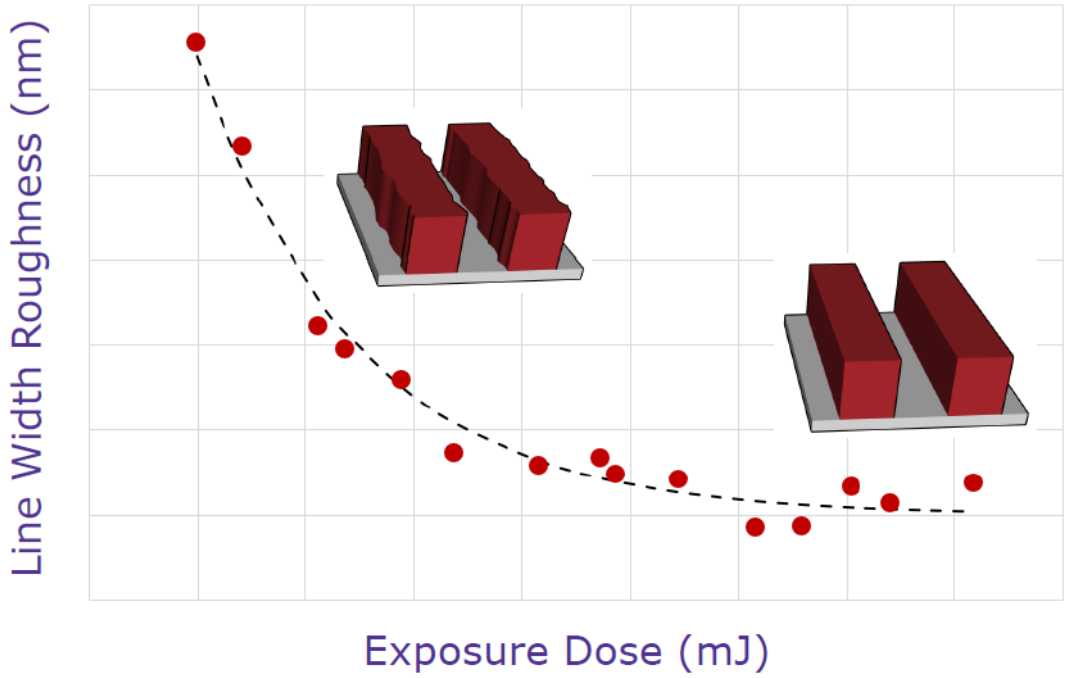


Eric A. Karl "Evolutions in technology enabling the AI era", Proc. SPIE 13425, DTCO and Computational Patterning IV, 1342502 (23 April 2025); https://doi.org/10.1117/12.3056887

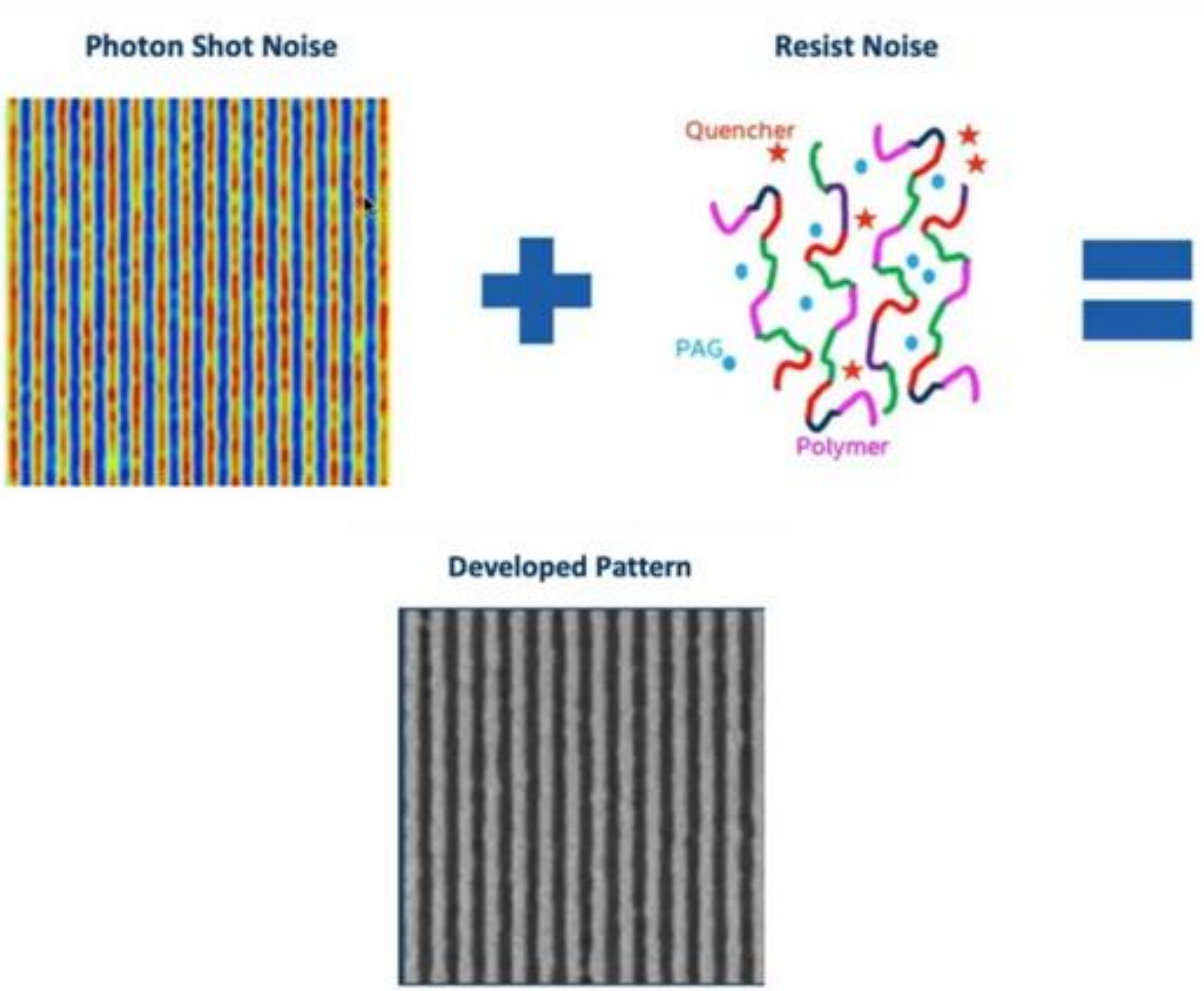
One limitation of EUV lithography (*): line edge roughness

EUV Lithography

LWR Dependency on Exposure Dose



10 Semiconductor Materials Webinar Series | Overcoming EUV Lithography Barriers through DSA technology | 12.04.2022



(*) Performance as of today:
Resolution: 8 nm. Wafers per hour: 185. Overlay alignment: 1.2 nm.

Han, E. et al. "DSA materials and processes development for ≤ P24 EUV resist L/S pattern rectification," Proc. SPIE 12956 (2024)

April 18, 2024

Intel's 14A Magic Bullet: Directed Self-Assembly (DSA) // How High-NA EUV can be economically viable at the 1.4nm process node

13 minutes

7 comments

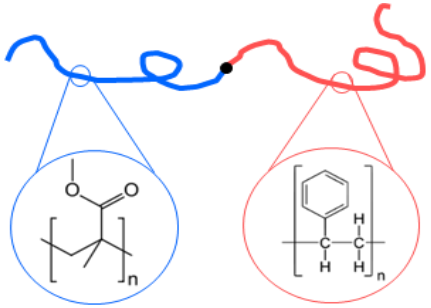
By Dylan Patel and Jeff Koch

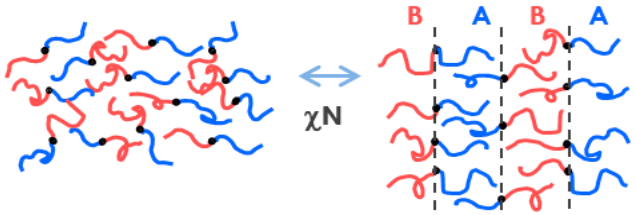
https://semianalysis.com/

General concepts about DSA

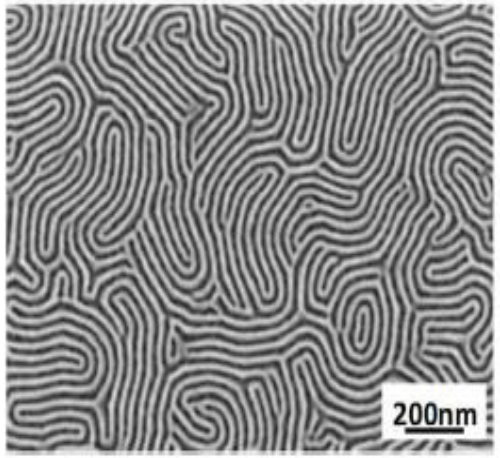
Microphase-separation of block copolymers

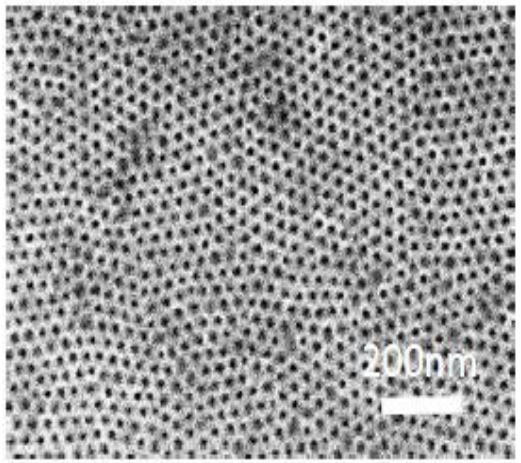
- Occurs on the nanoscale, since the two blocks are covalently bound





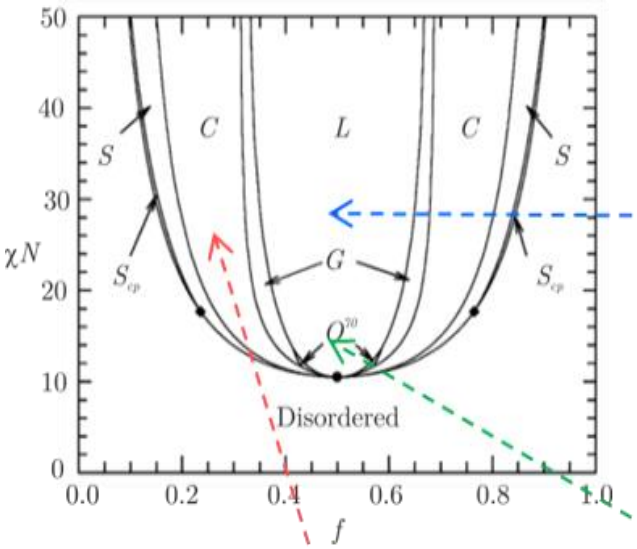
Disorder-order transition

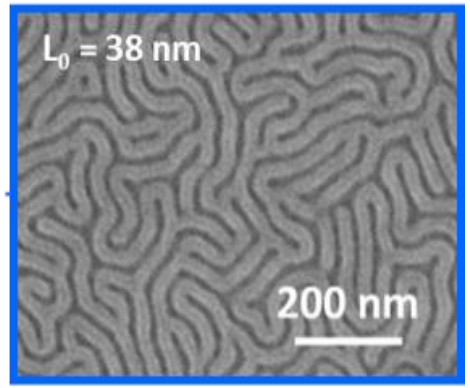


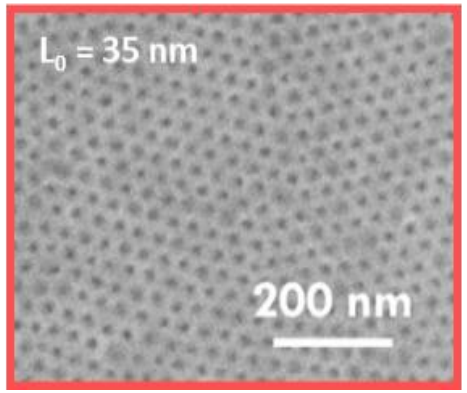


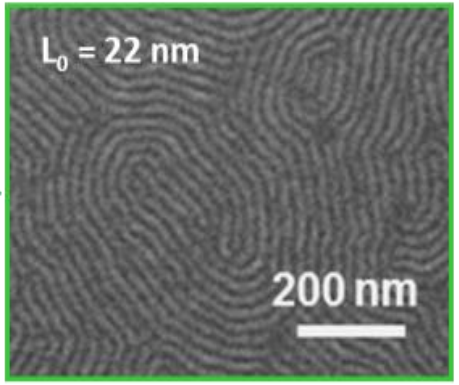
Morphology of PS-b-PMMA thin films

- The relative composition between blocks and their molecular weight dictates morphology and feature size







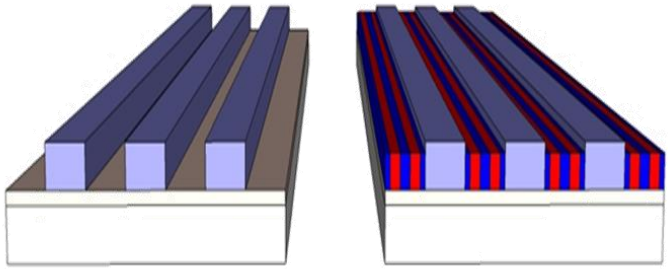


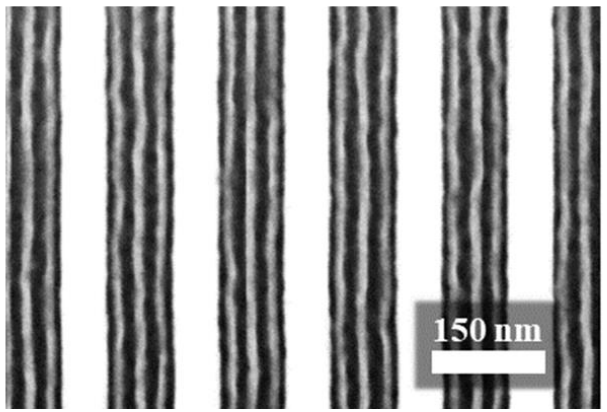
24

Directed self-assembly: guiding patterns

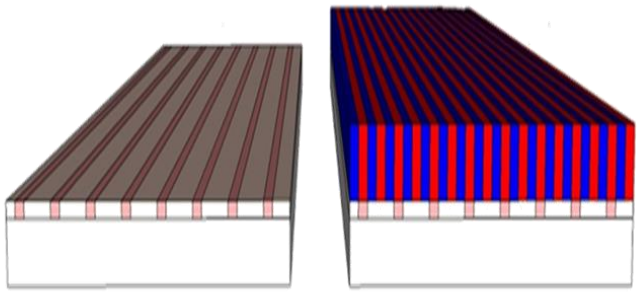
Line/space density multiplication

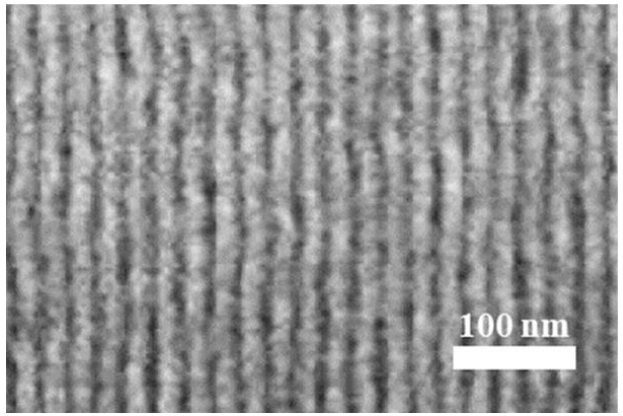
Graphoepitaxy





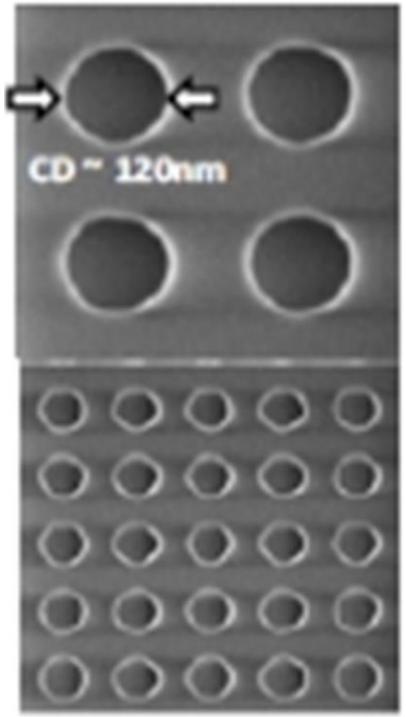
Chemoepitaxy

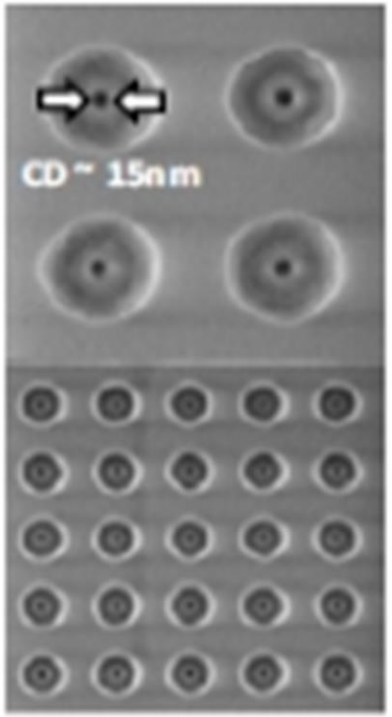




S. Gottlieb, D. Kazazis, I. Mochi, L. Evangelio, M. Fernández-Regúlez, Y. Ekinci, F. Perez-Murano
SPIE Advanced Lithography, San José. (2017)

Contact shrink

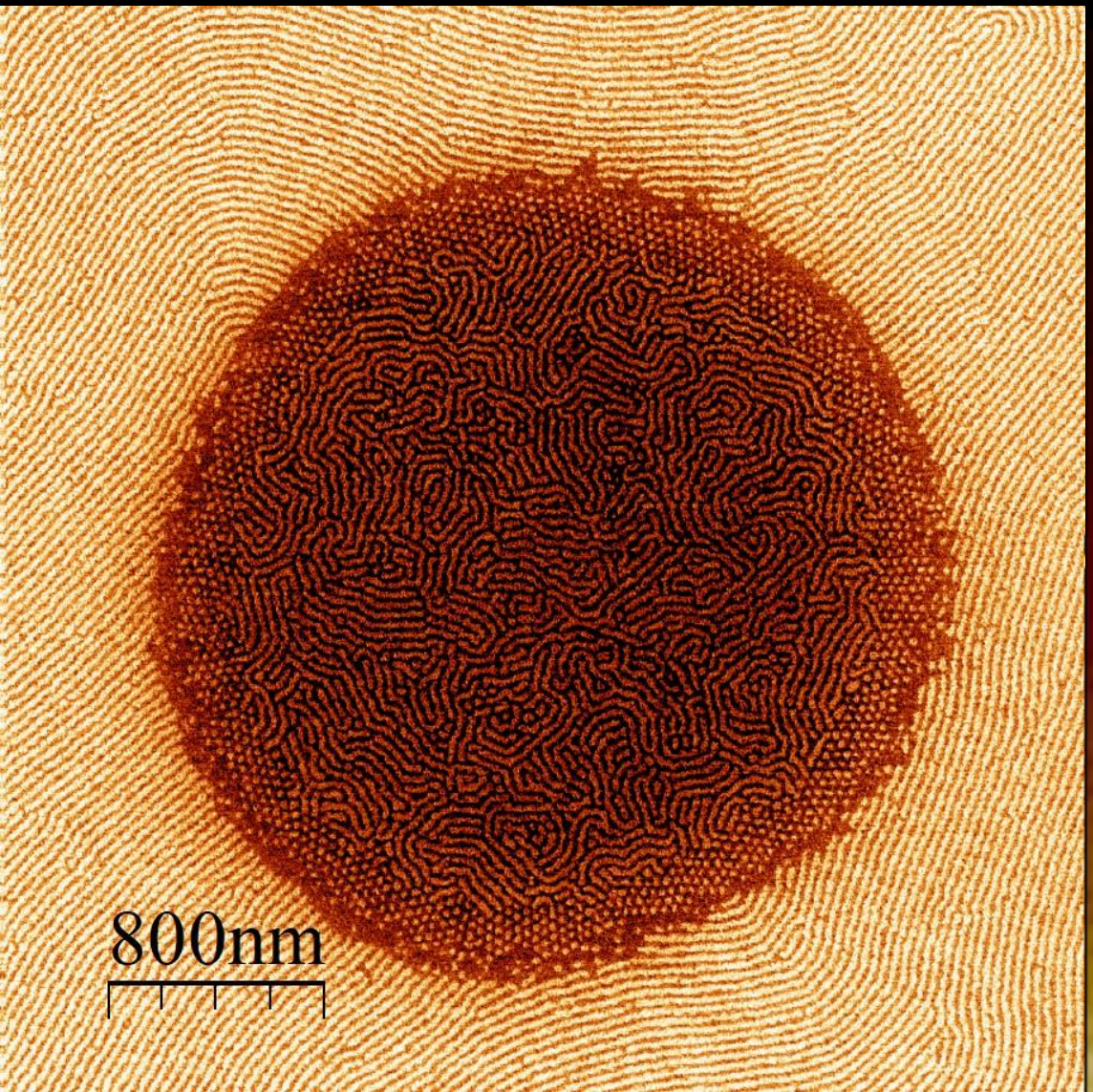


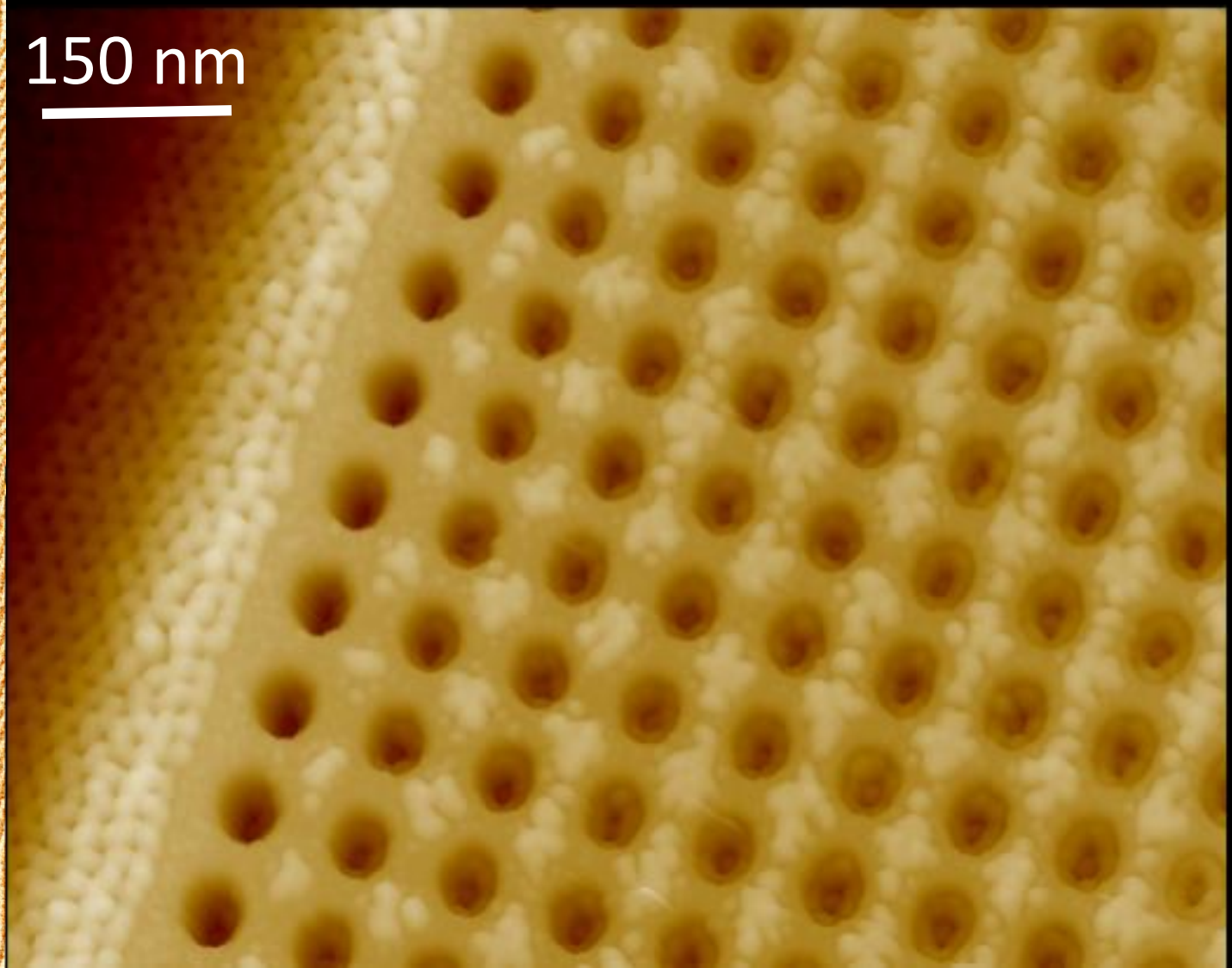


Tiron, R. et al. , “The potential of BCP’s DSA for contact hole shrink and contact multiplication”, Proc. SPIE, 8680, p. 868012 (2013)

25

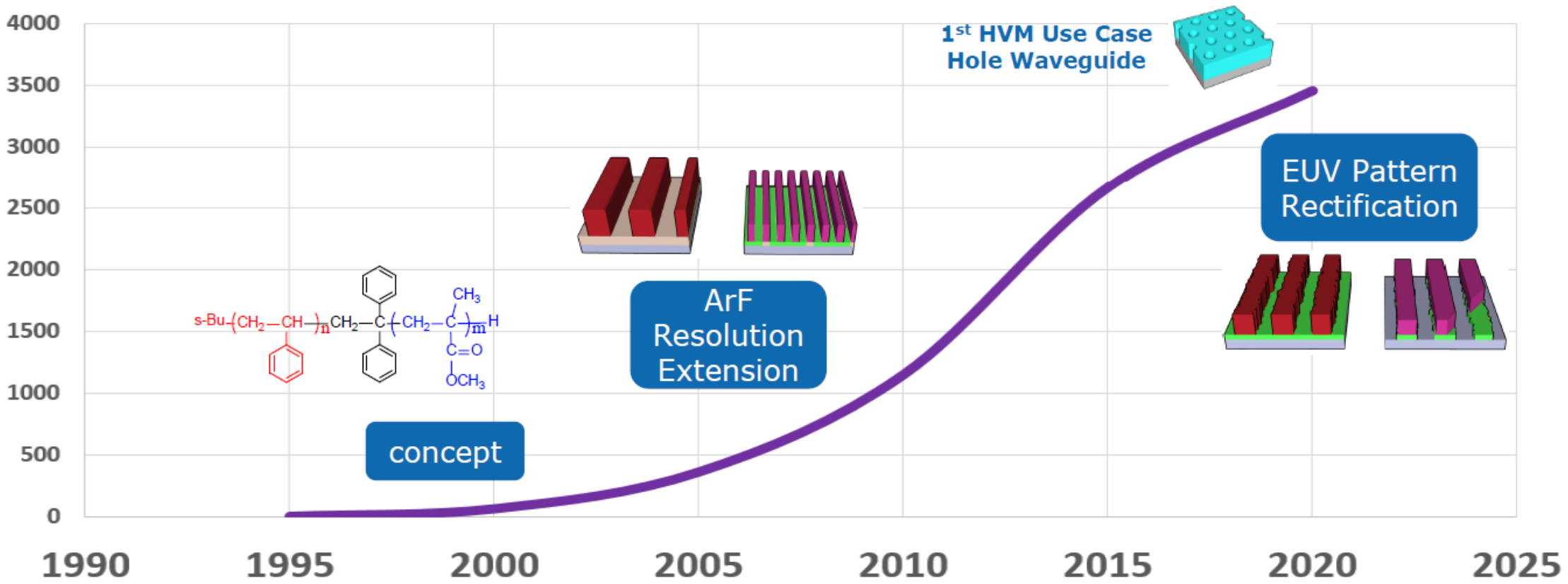
Directed self assembly of block copolymer thin films



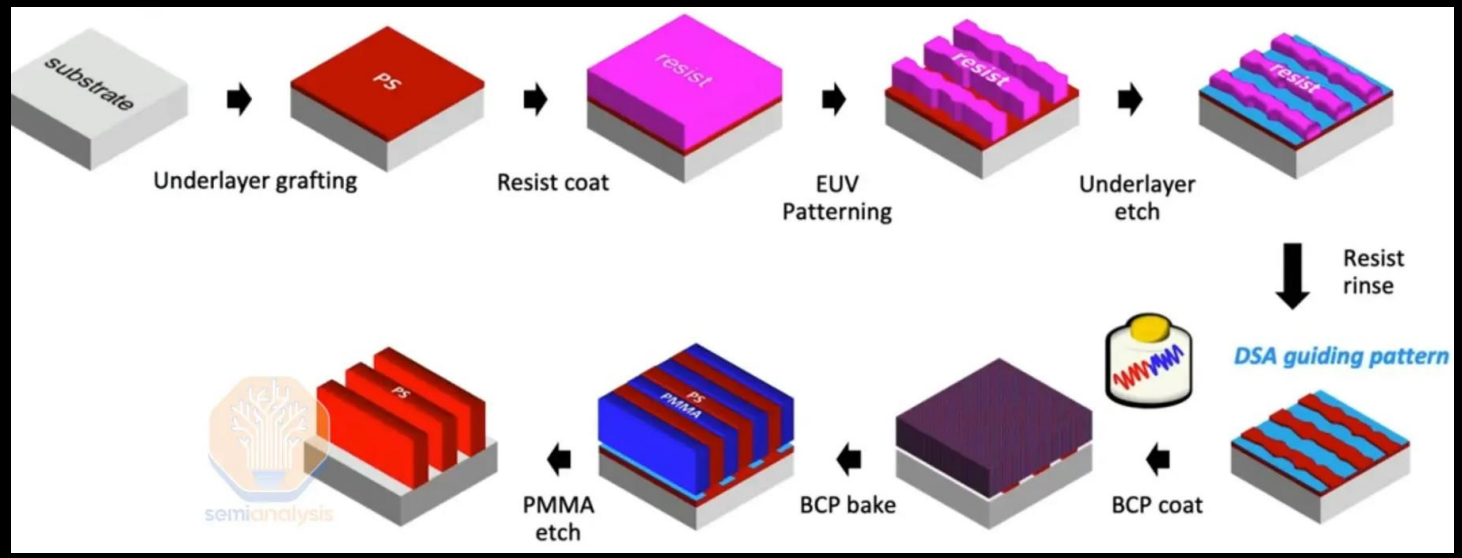


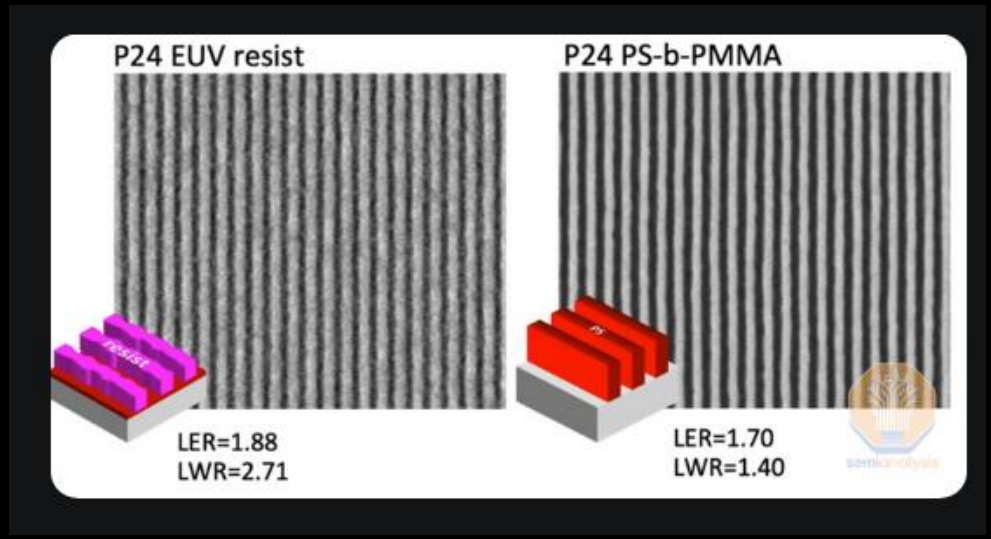
Historical Context
Directed Self-Assembly Applications

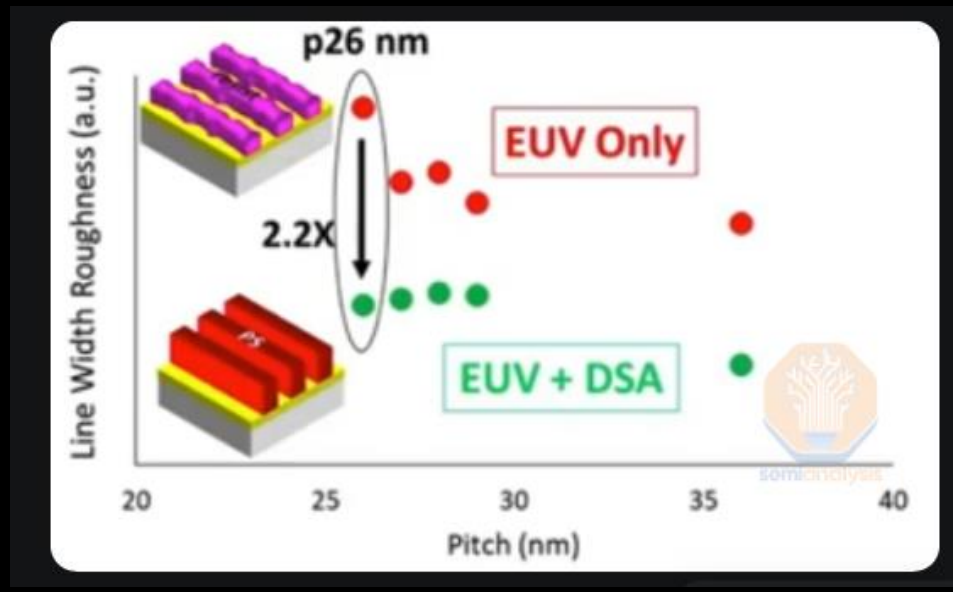
DSA Technical Literature & Articles (5yr increment sum)



Line edge roughness improvement by DSA





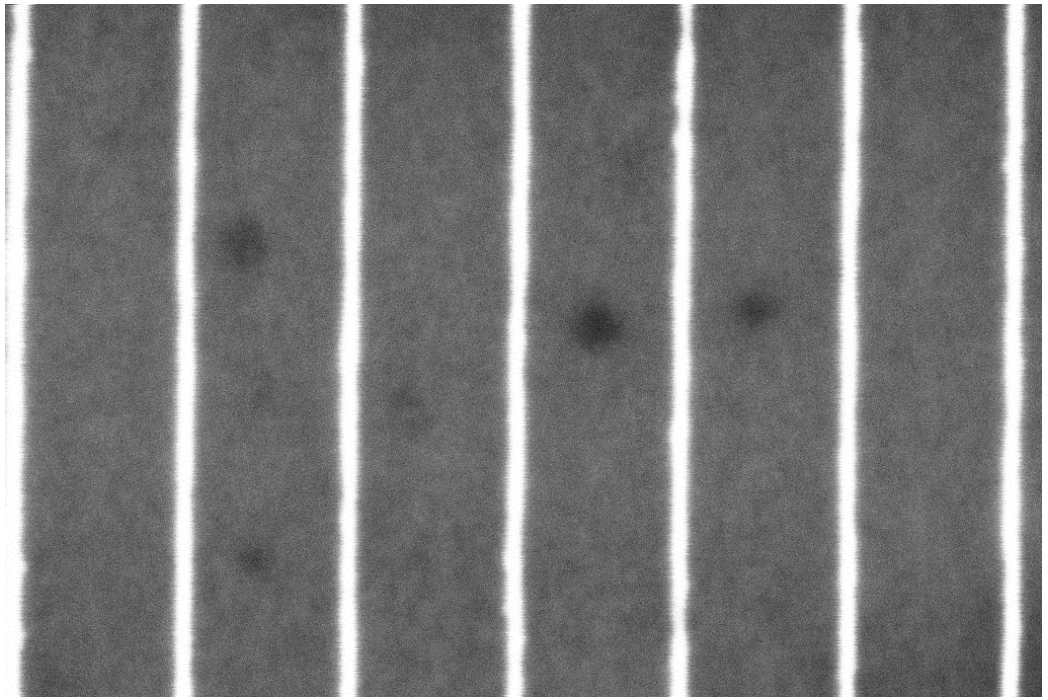


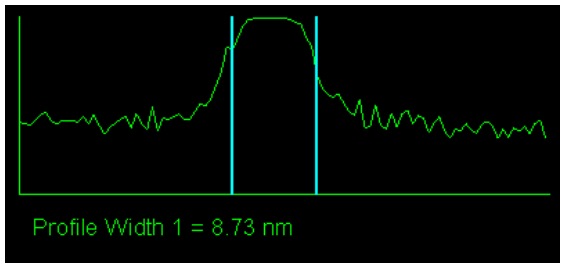
Han, E. et al. "DSA materials and processes development for ≤ P24 EUV resist L/S pattern rectification," Proc. SPIE 12956 (2024)

https://semianalysis.com/

DSA for line/space: high resolution guiding patterns

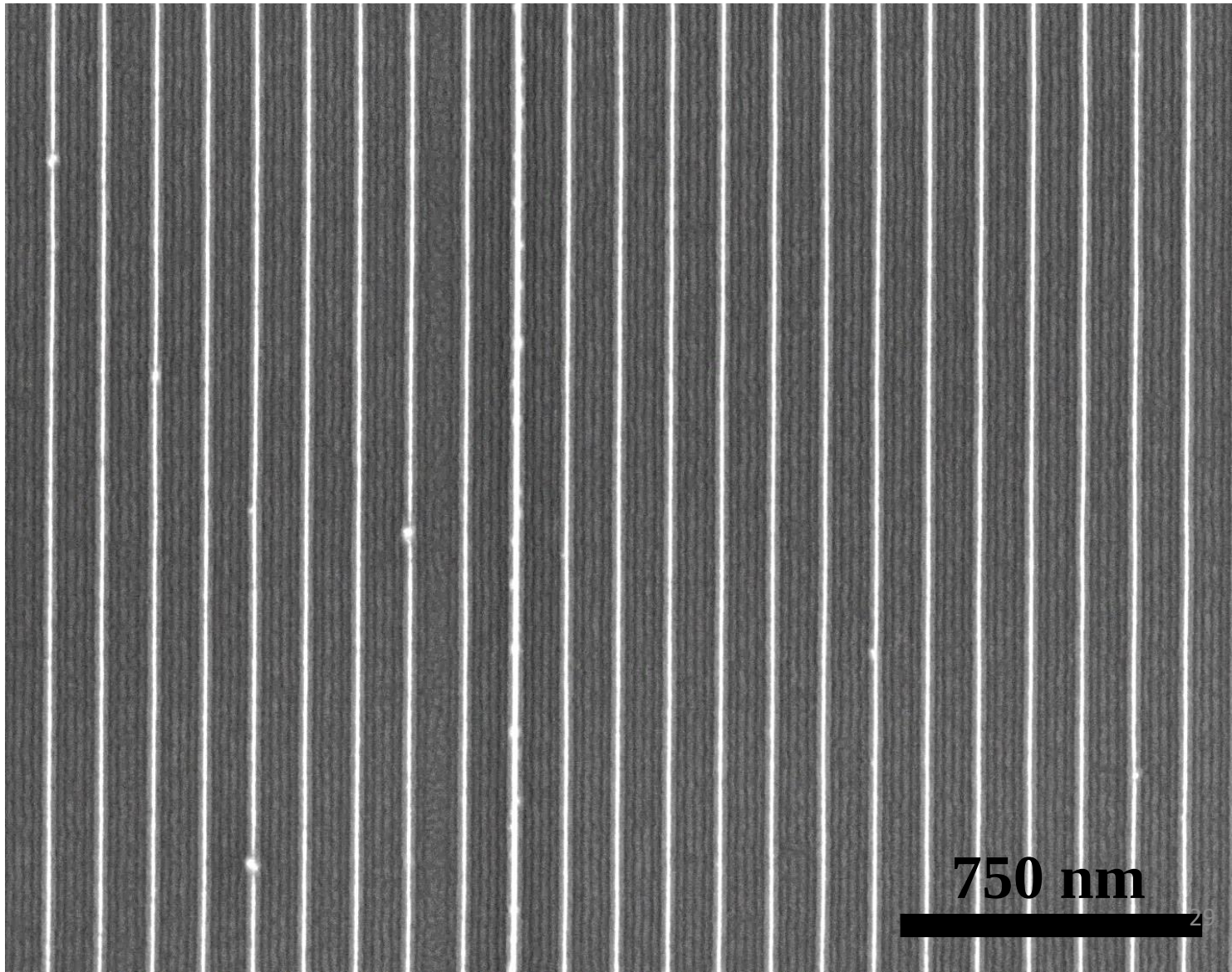
High resolution guiding patterns by EBL



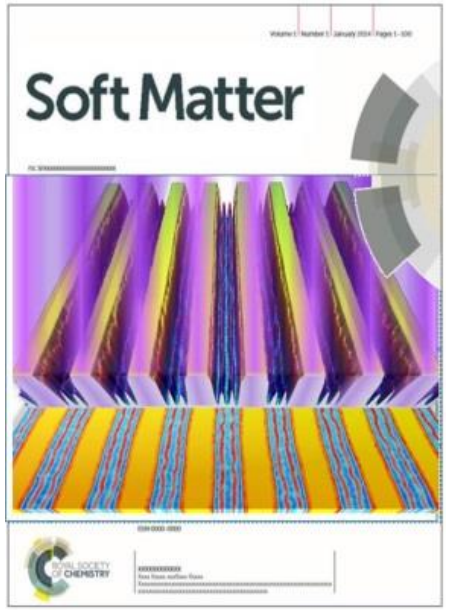


Sub-10 nm line width demonstrated
Pitch: 90 nm)

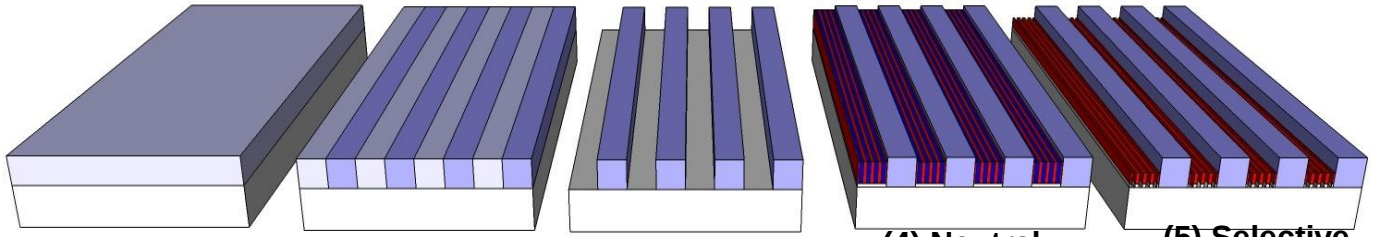
Gottlieb et al., 2018, Soft Matter, 14, 6799(808)



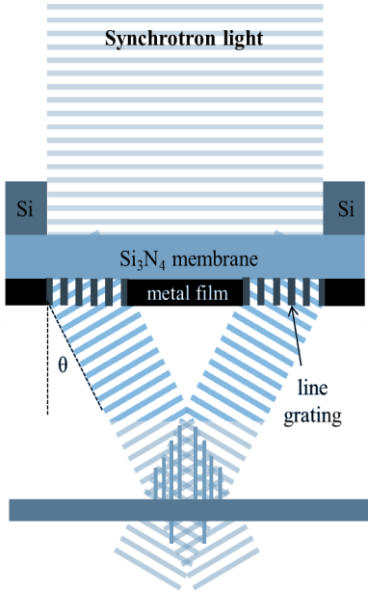
Nano-confinement and defectivity

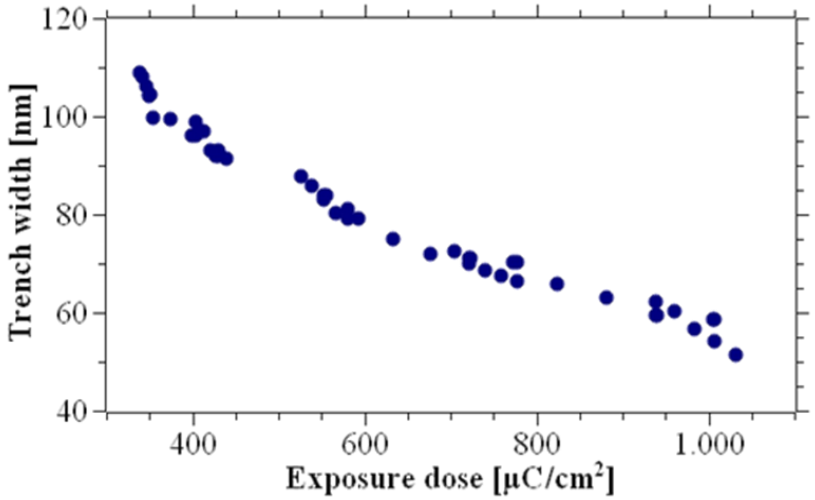


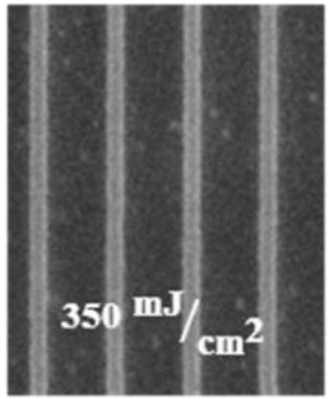
Gottlieb et al., 2018, Soft Matter, 14, 6799(808)

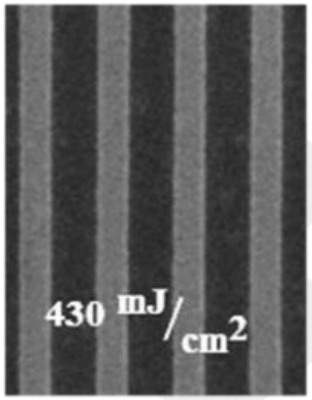


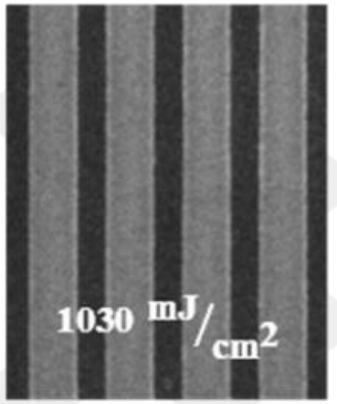
(1) HSQ deposition (2) EUV exposure (3) Development (4) Neutral brush + DSA (5) Selective PMMA removal

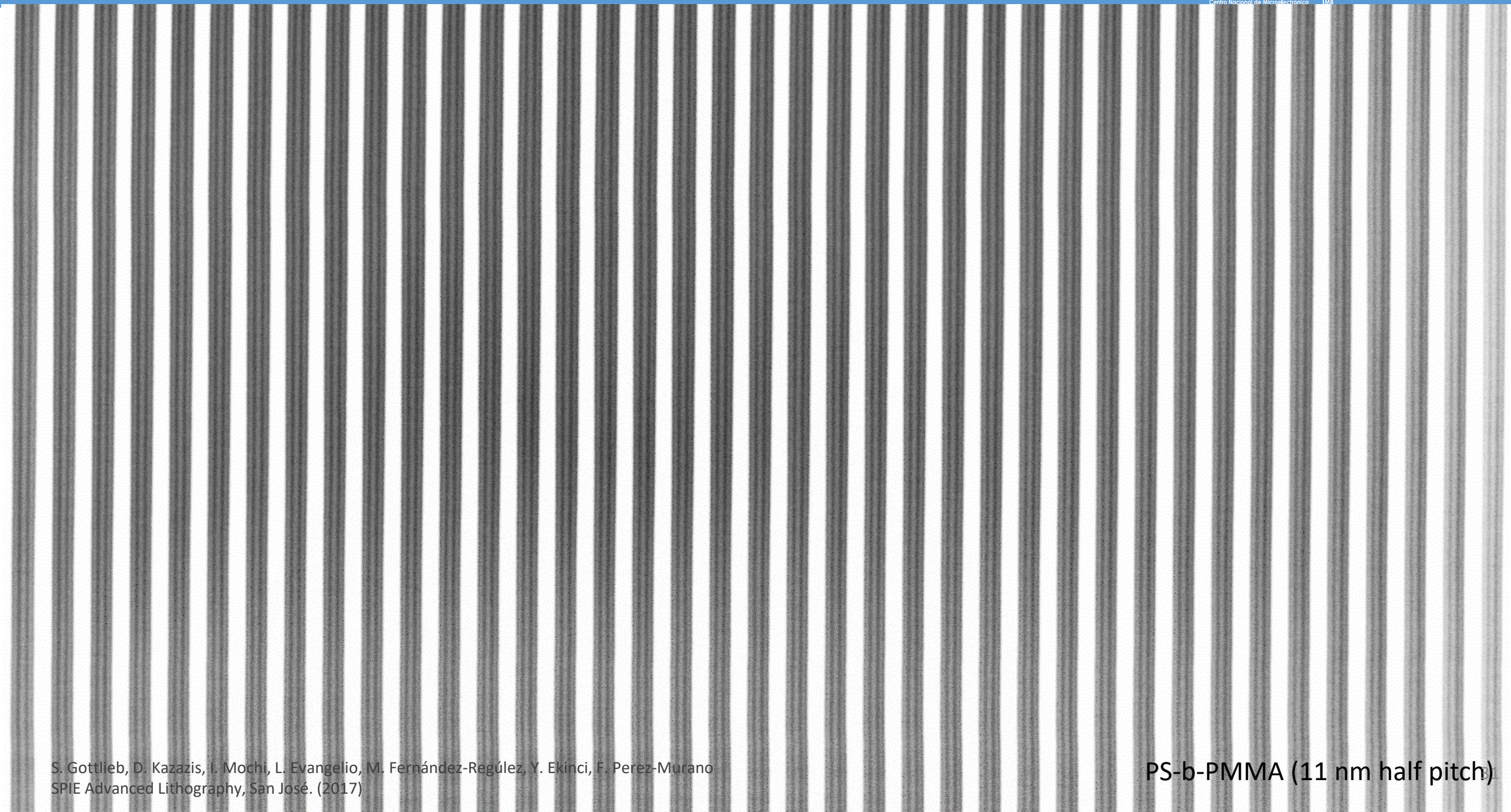








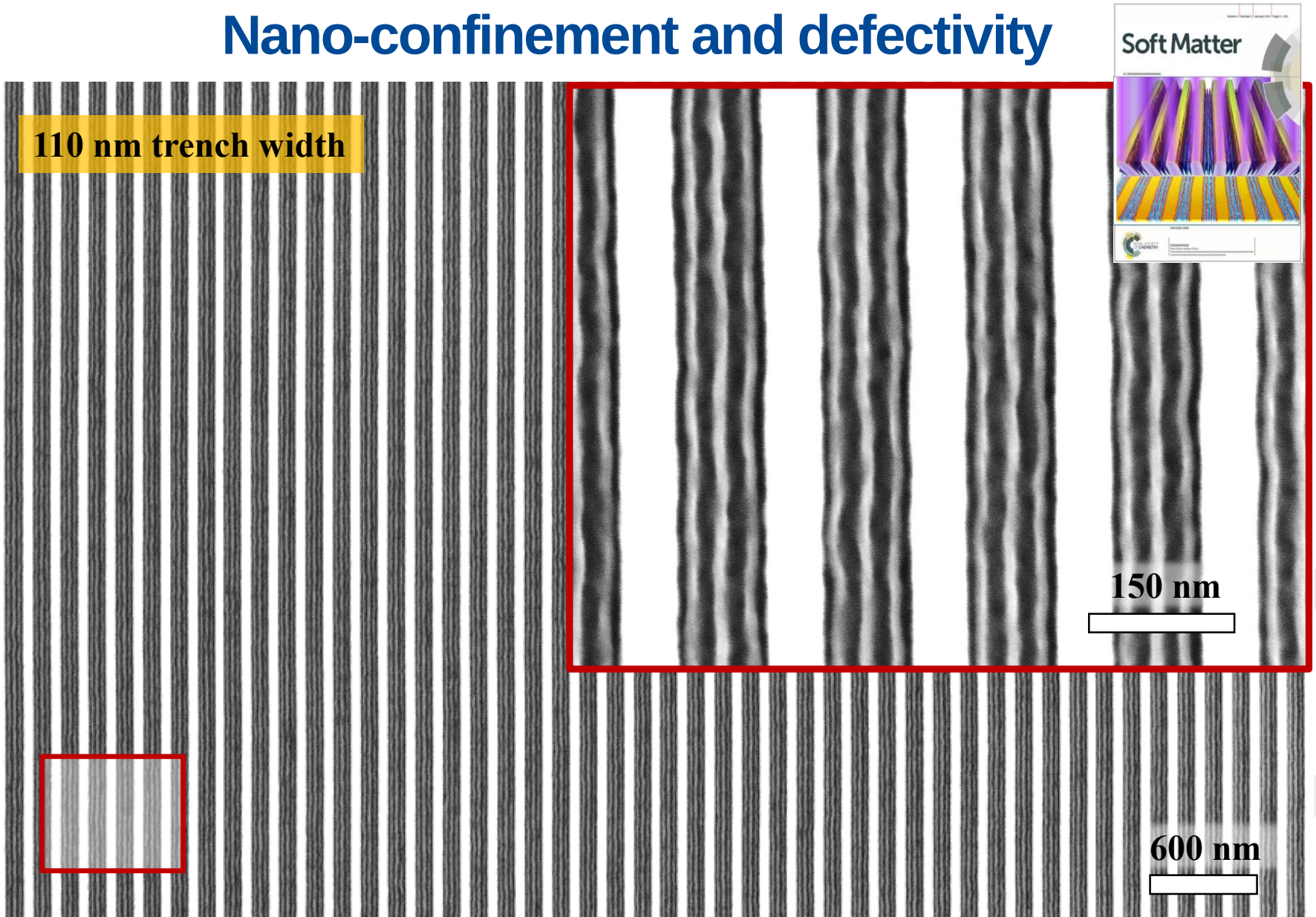




S. Gottlieb, D. Kazazis, I. Mochi, L. Evangelio, M. Fernández-Regúlez, Y. Ekinci, F. Perez-Murano
SPIE Advanced Lithography, San José. (2017)

PS-b-PMMA (11 nm half pitch)

Nano-confinement and defectivity



Semiconductor spin qubits

- The **spin of an electron or a nucleus** functions as an excellent qubit.
- It provides **a natural two-level system that is insensitive to electric fields, leading to long quantum coherence times.**
- This coherence survives when the spin is isolated and controlled within nanometer-scale, lithographically fabricated semiconductor devices, enabling the existing microelectronics industry to help advance spin qubits into a **scalable technology.**

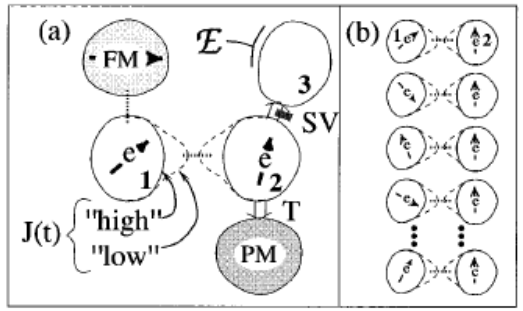
Two seminal proposals

PHYSICAL REVIEW A VOLUME 57, NUMBER 1 JANUARY 1998

Quantum computation with quantum dots

Daniel Loss[1,2,*] and David P. DiVincenzo[1,3,†]
[1]*Institute for Theoretical Physics, University of California, Santa Barbara, Santa Barbara, California 93106-4030*
[2]*Department of Physics and Astronomy, University of Basel, Klingelbergstrasse 82, 4056 Basel, Switzerland*
[3]*IBM Research Division, T.J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598*
(Received 9 January 1997; revised manuscript received 22 July 1997)

We propose an implementation of a universal set of one- and two-quantum-bit gates for quantum computation using the spin states of coupled single-electron quantum dots. Desired operations are effected by the gating of the tunneling barrier between neighboring dots. Several measures of the gate quality are computed within a recently derived spin master equation incorporating decoherence caused by a prototypical magnetic environment. Dot-array experiments that would provide an initial demonstration of the desired nonequilibrium spin dynamics are proposed. [S1050-2947(98)04501-6]

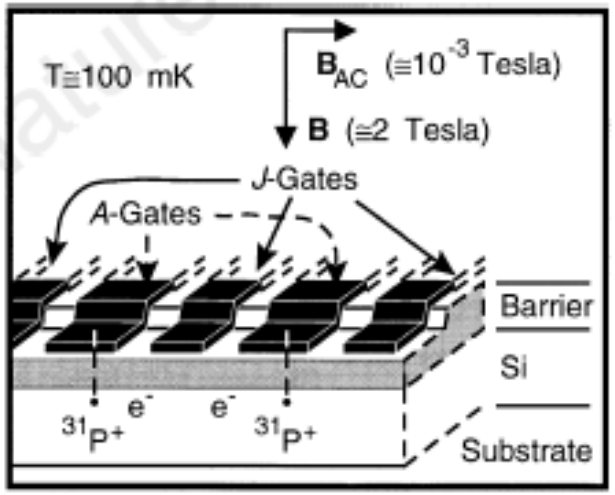


Loss- DiVincenzo
PRL. 1998

A silicon-based nuclear spin quantum computer

B. E. Kane
Semiconductor Nanofabrication Facility, School of Physics, University of New South Wales, Sydney 2052, Australia

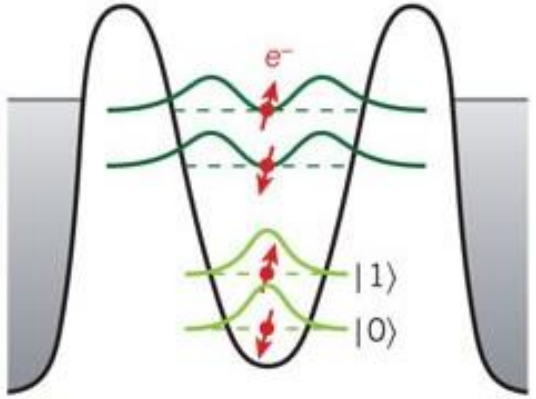
Quantum computers promise to exceed the computational efficiency of ordinary classical machines because quantum algorithms allow the execution of certain tasks in fewer steps. But practical implementation of these machines poses a formidable challenge. Here I present a scheme for implementing a quantum-mechanical computer. Information is encoded onto the nuclear spins of donor atoms in doped silicon electronic devices. Logical operations on individual spins are performed using externally applied electric fields, and spin measurements are made using currents of spin-polarized electrons. The realization of such a computer is dependent on future refinements of conventional silicon electronics.

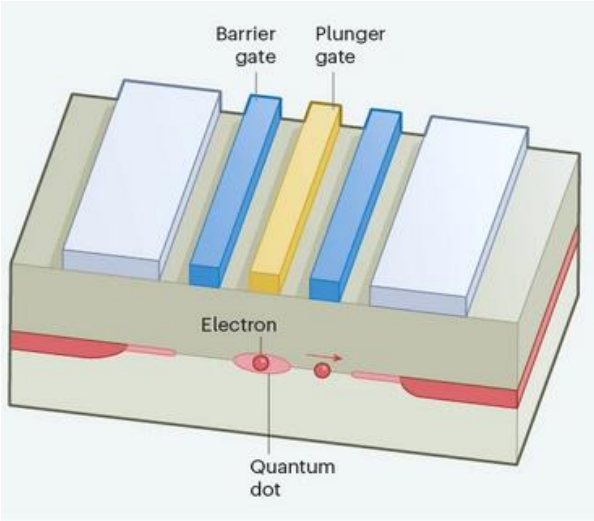


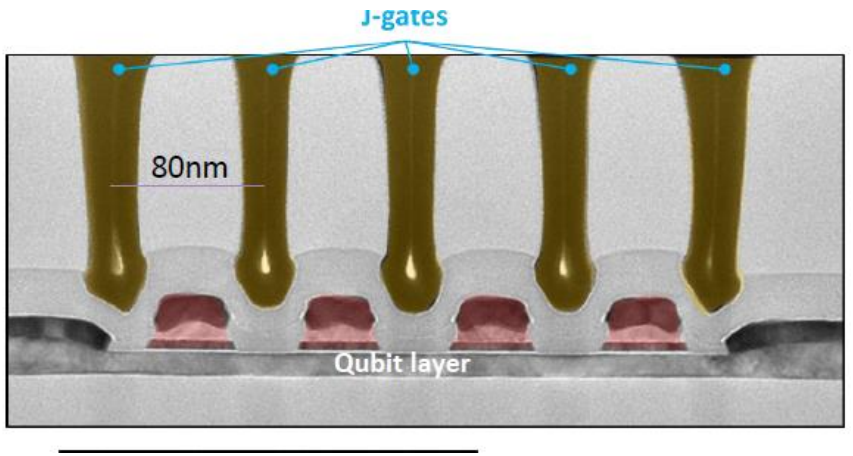
Kane
Nature. 1998

SEMICONDUCTOR SPIN QUBITS

Electrostatic quantum dots (spin of the electron)

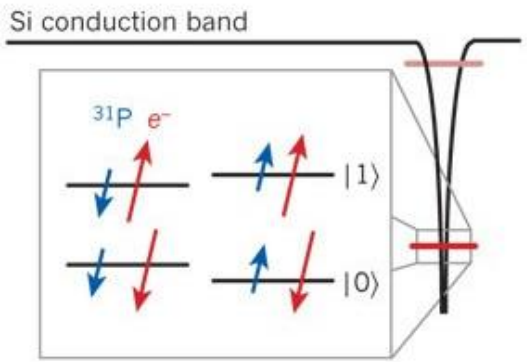


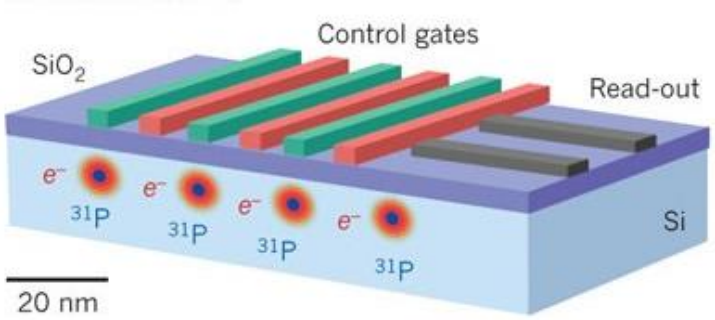


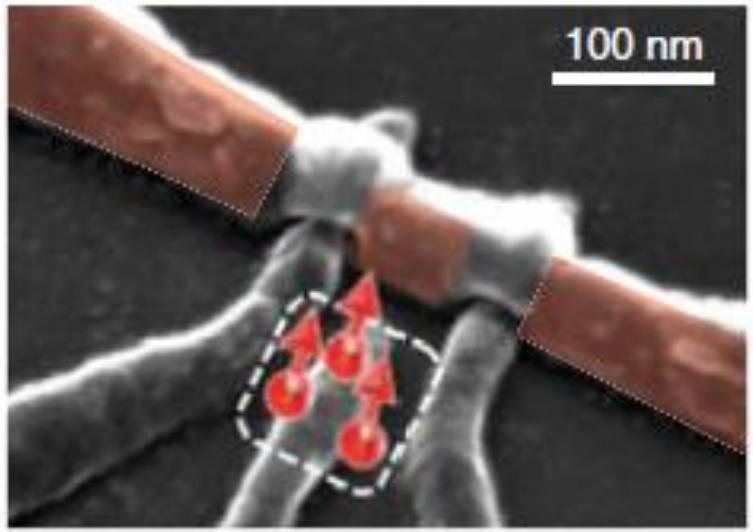


Bédérrecats. 2021

Single dopant (nuclear spin)

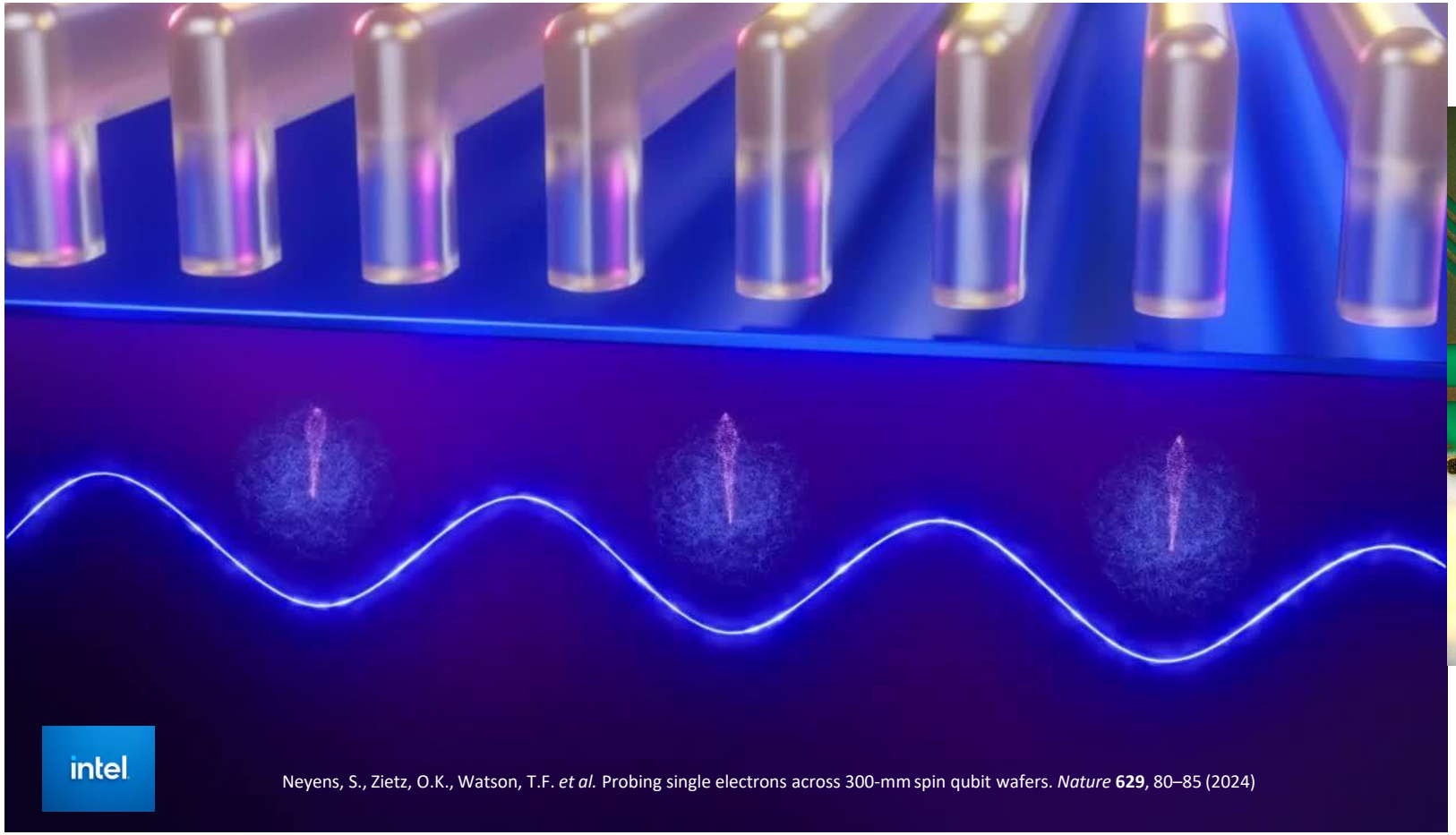






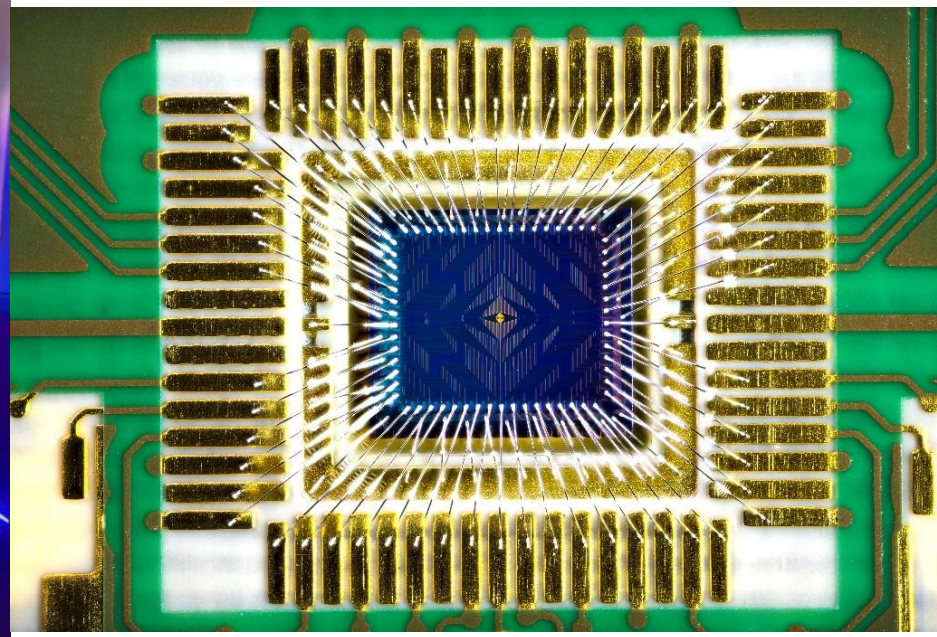
Morello. 2010

Semiconductor spin qubits



Neyens, S., Zietz, O.K., Watson, T.F. *et al.* Probing single electrons across 300-mm spin qubit wafers. *Nature* **629**, 80–85 (2024)

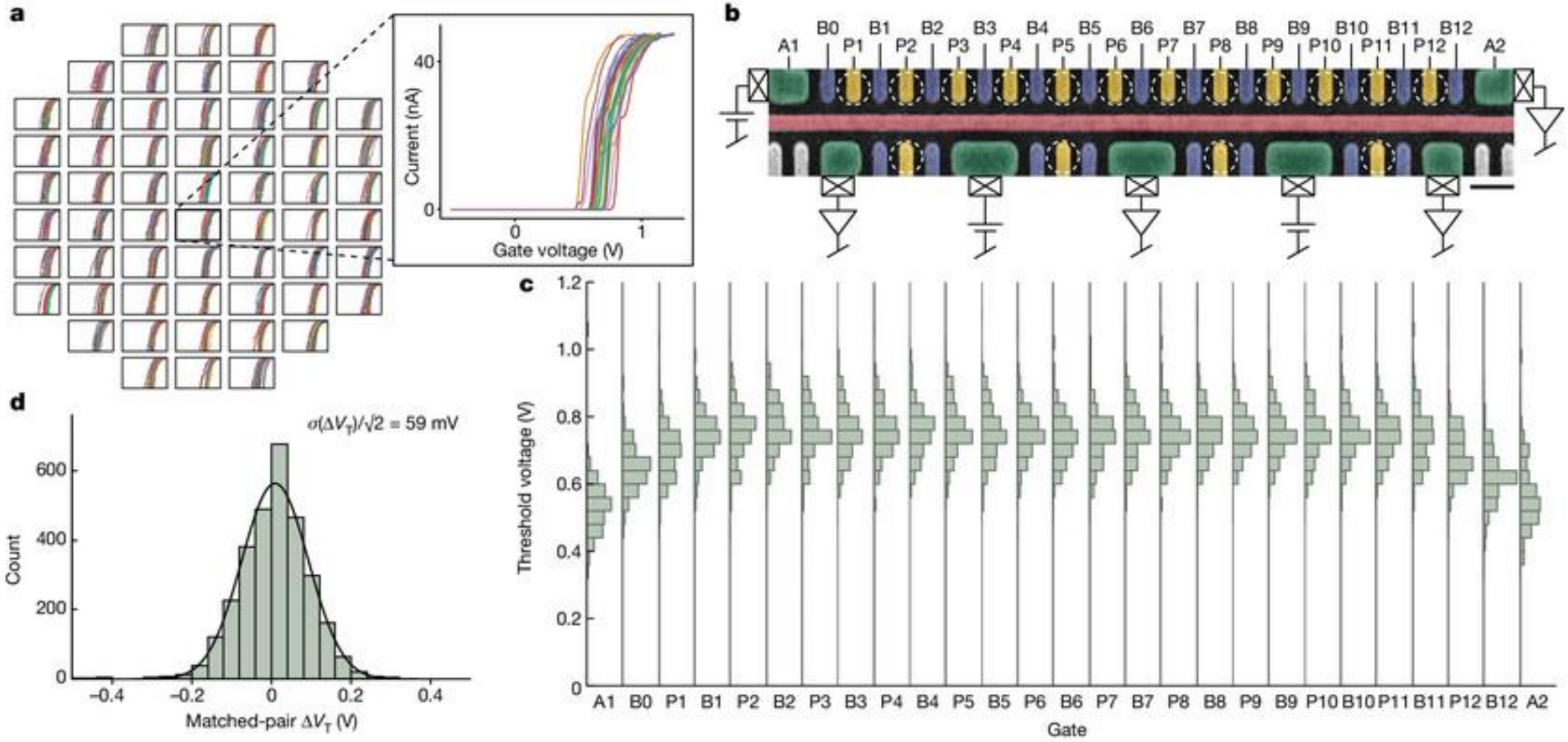
Tunnel Falls (2023)



a 12-qubit silicon chip

https://newsroom.intel.com/new-technologies/quantum-computing-chip-to-advance-research

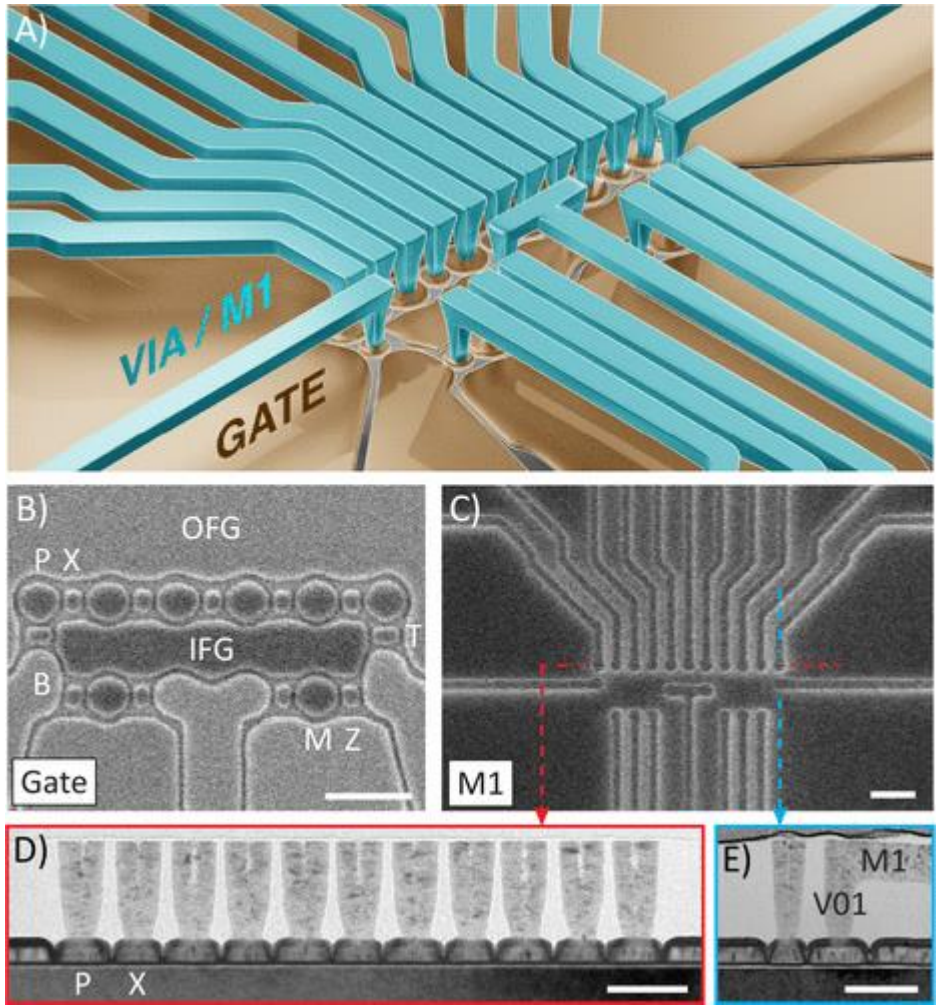
- Industry-compatible process to fabricate spin qubit devices, Intel's D1 factory,
- 300-mm cryogenic probing process to collect high-volume data on spin qubit devices across full wafers
- All patterning is done with extreme ultraviolet lithography, gate pitches from 50 to 100 nm.
- The fabrication is based on fundamental industry techniques of deposition, etch and chemical-mechanical polish



Tiled array of *I*–*V* curves taken on 12QD devices across a wafer

Neyens, S., Zietz, O.K., Watson, T.F. *et al.* Probing single electrons across 300-mm spin qubit wafers. *Nature* **629**, 80–85 (2024)

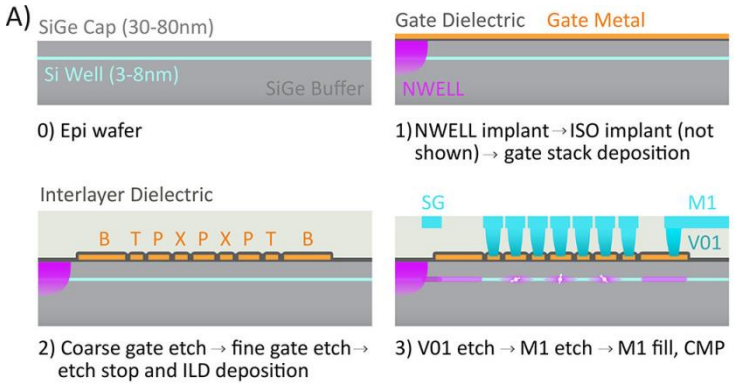
The problem of contacting a dense array of gates

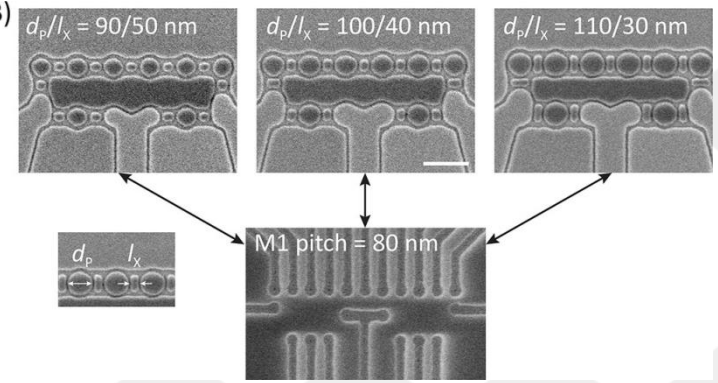


All gates are patterned simultaneously on the same plane (i.e., uniplanar);

Back-end-of-line (BEOL) interconnect layers, in which vertical vias directly contact active gates and then spans to macroscopic routing 10−50 µm away

The requirements for e-beam overlay between V01-gate and M1-V01 layers are approximately 5−15 nm,





Wonill Ha et al Nano Lett. 2022, 22, 3, 1443–1448

Scale bar:100 nm

HRL LABORATORIES

E-beam lithography repeatability

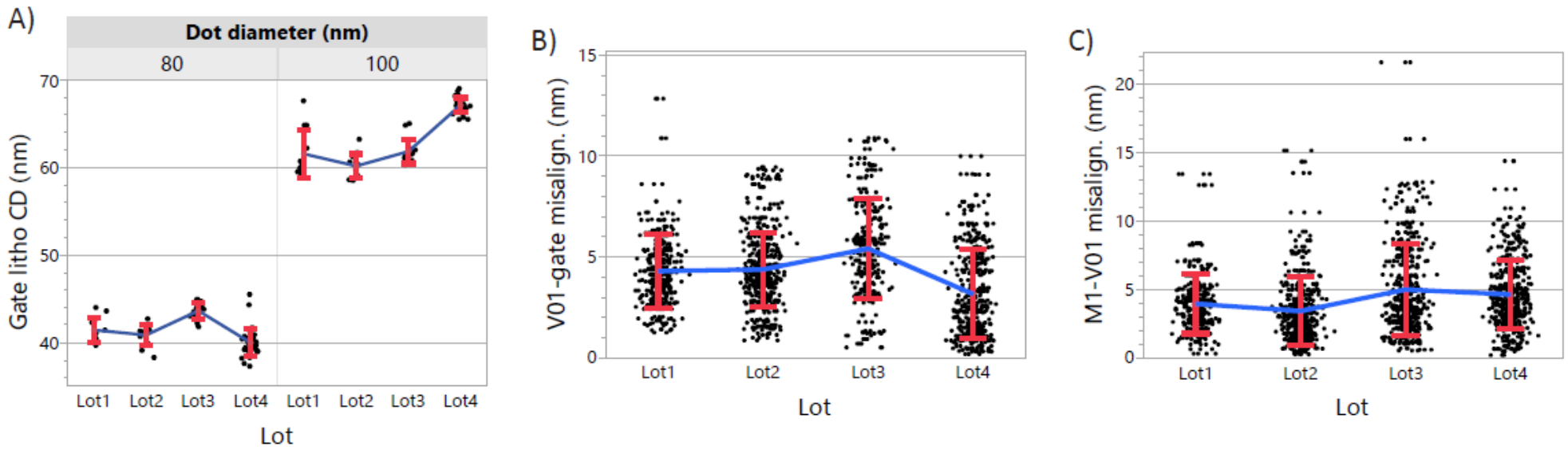


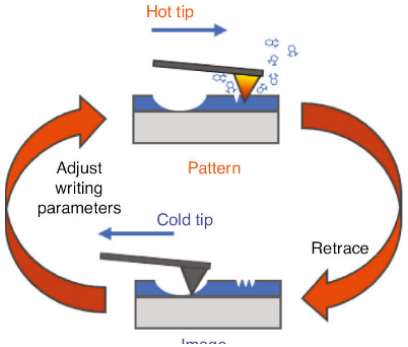
Figure S3: (A) Plunger gate CD after e-beam lithography for two different dot diameters across four lots. (B) Magnitude of misalignment between V01 and gate levels across same four lots as in (A). (C) Magnitude of misalignment between M1 and V01 levels across same four lots as in (A). In all plots, blue lines connect lot means and red bars are one standard deviation from the mean.

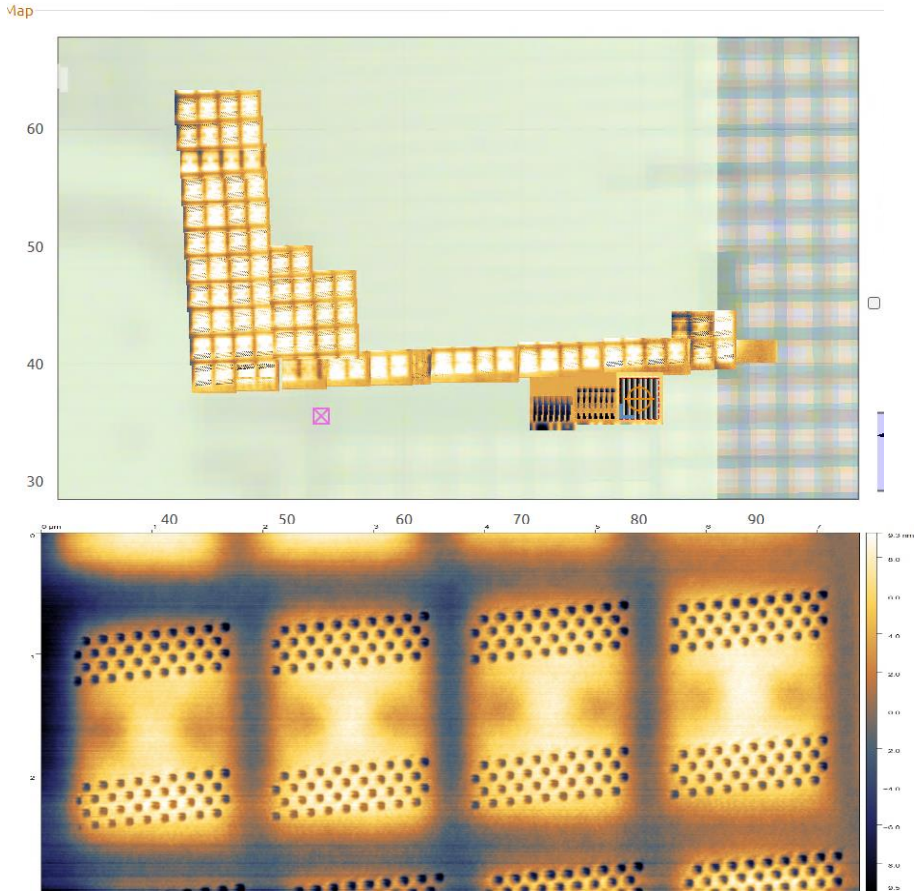
A Flexible Design Platform for Si/SiGe Exchange-Only Qubits with Low Disorder
Wonill Ha, Sieu D. Ha, Maxwell D. Choi, Yan Tang, Adele E. Schmitz, Mark P. Levendorf, Kangmu Lee, James M. Chappell, Tower S. Adams, Daniel R. Hulbert, Edwin Acuna, Ramsey S. Noah, Justine W. Matten, Michael P. Jura, Jeffrey A. Wright, Matthew T. Rakher, and Matthew G. Borselli
Nano Lett. 22 1443 (2022)

t-SPL and DSA for contact shrink with pattern placement accuracy

HEIDELBERG INSTRUMENTS

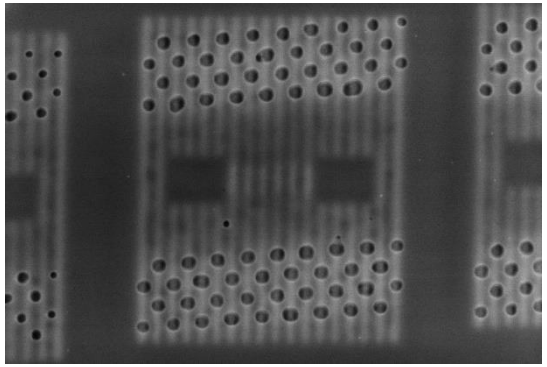
Qu-Pilot

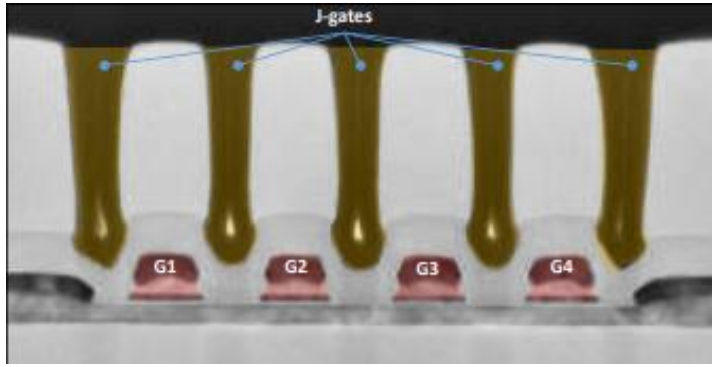


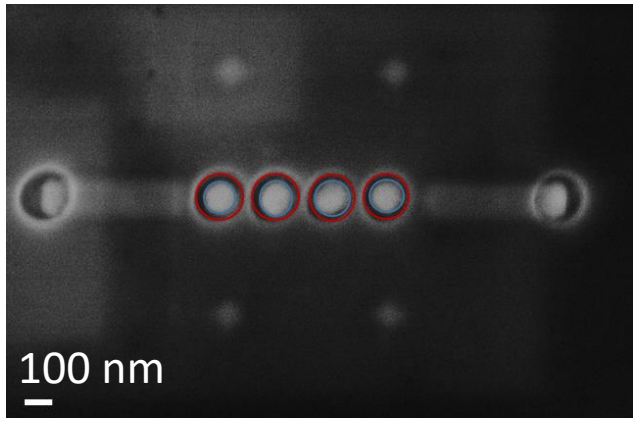


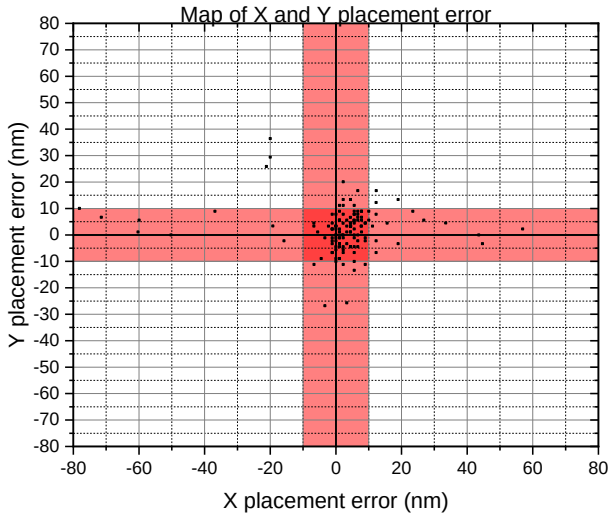
cea leti

T. Bedecarrats *et al.*, en *2021 IEEE International Electron Devices Meeting (IEDM)*





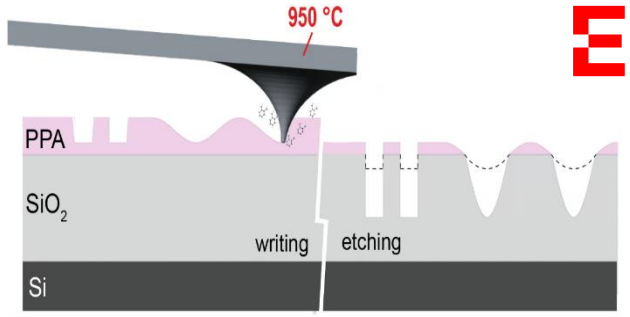


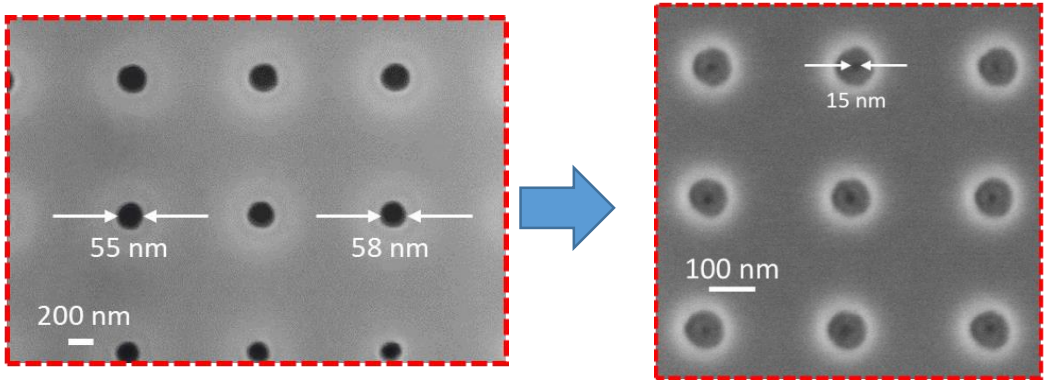


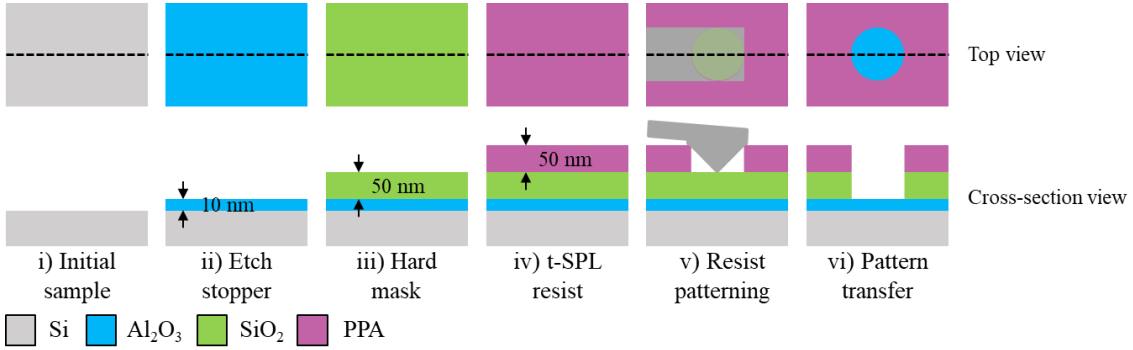
X placement error: μ=2.6 nm σ=3.6 nm

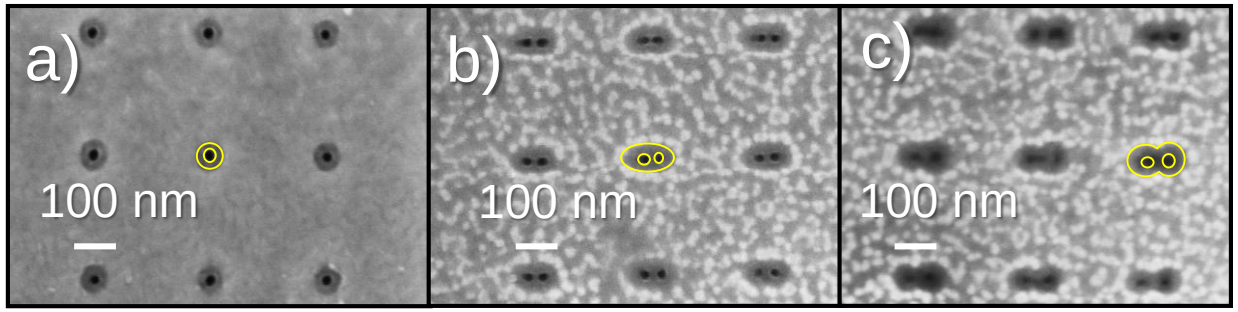
Y placement error: μ=1.3 nm σ=4.6 nm

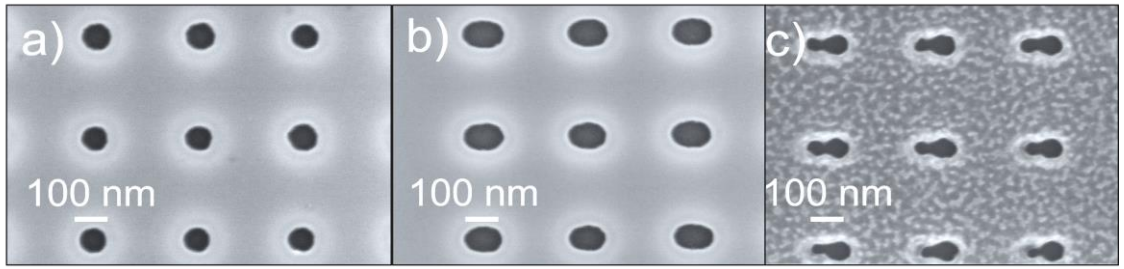
t-SPL and DSA for contact shrink with pattern placement accuracy

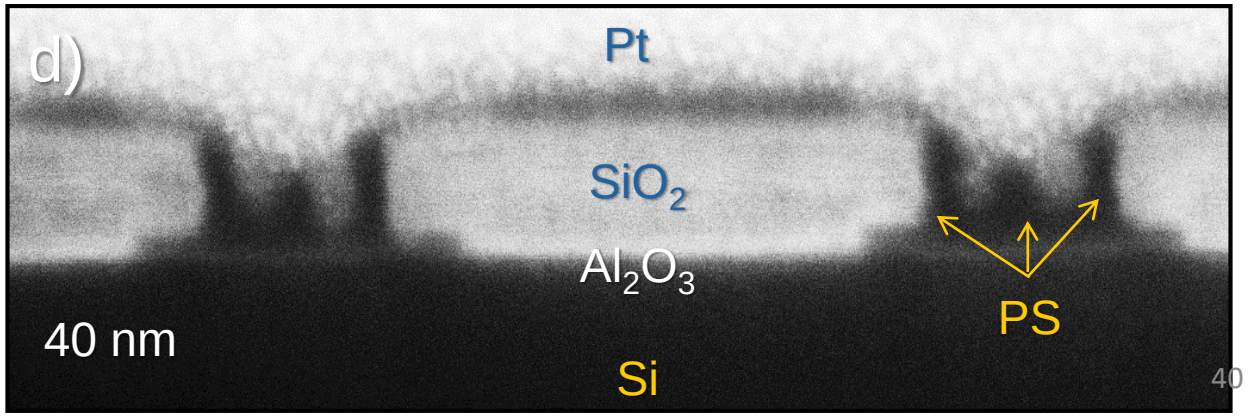






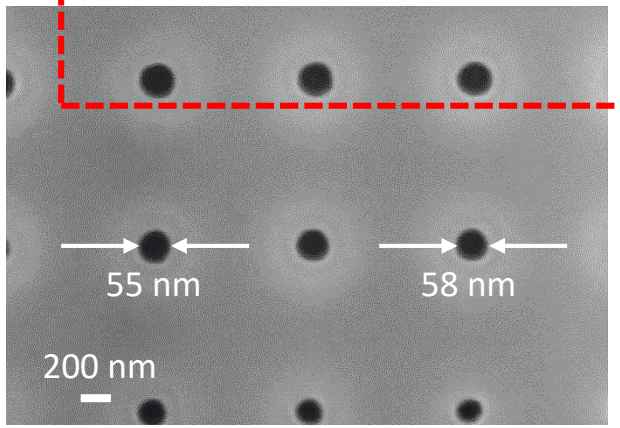


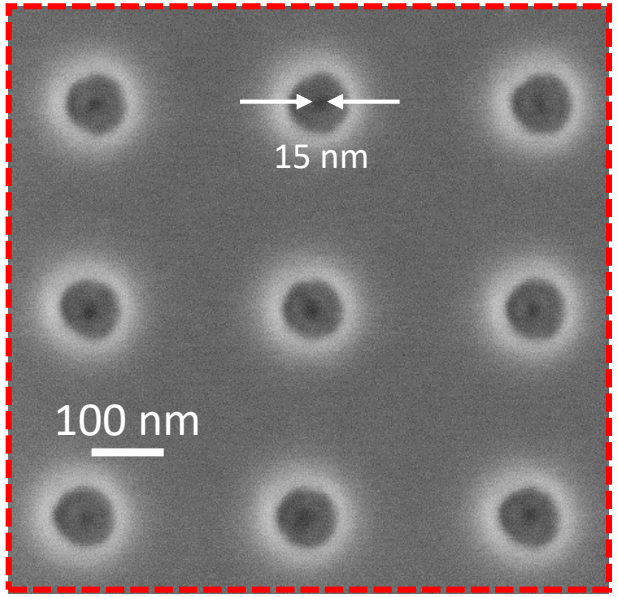


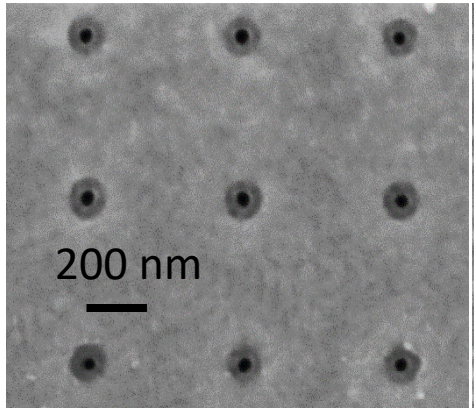


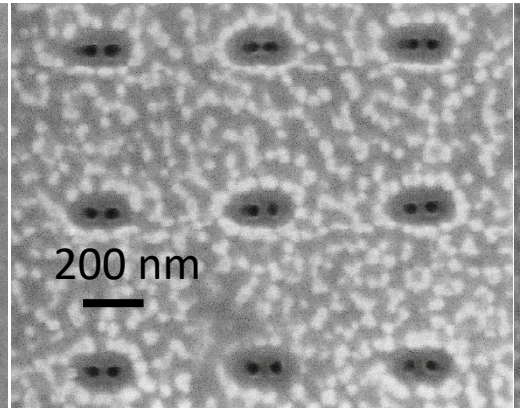
I. Uranga, E. Berke, et al. SPIE Advanced Lithography 2025

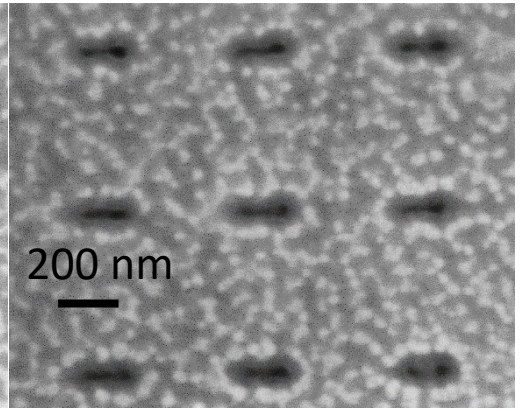
t-SPL and DSA for contact shrink with pattern placement accuracy

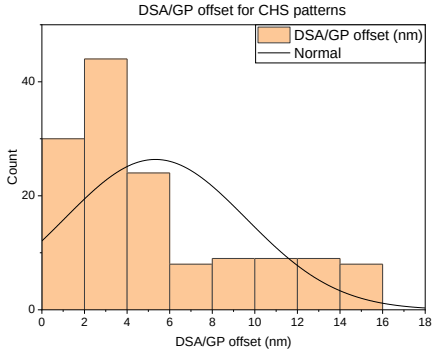


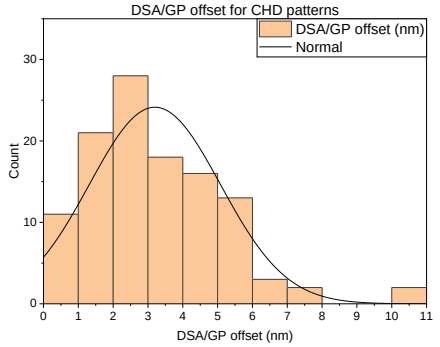


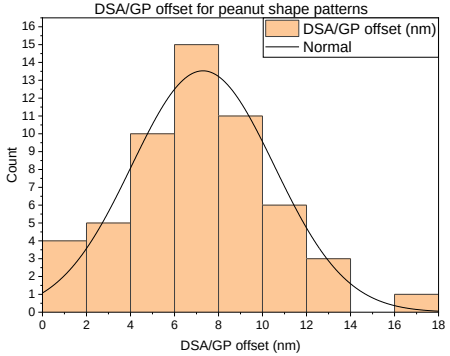






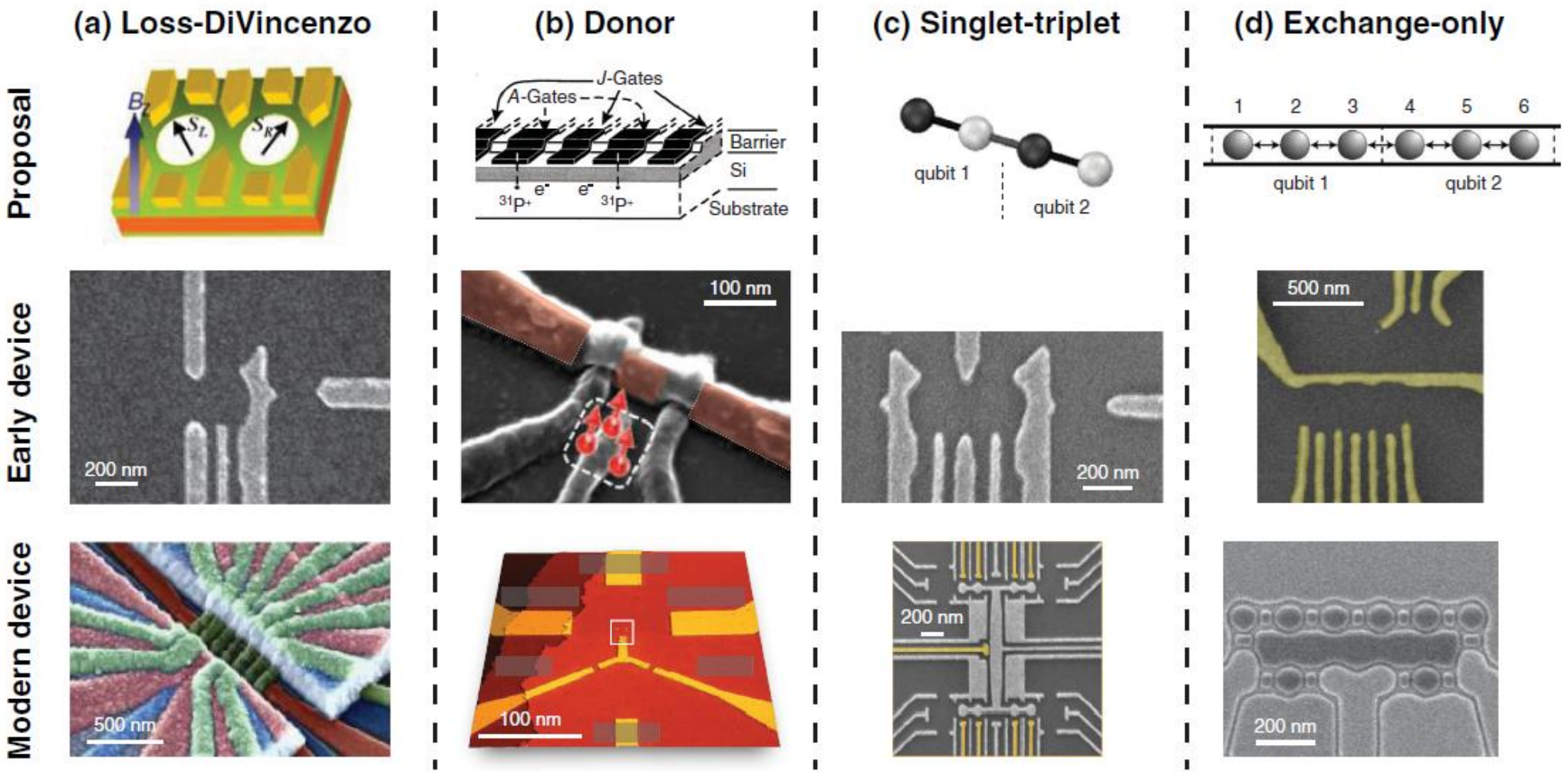






Quantum computing

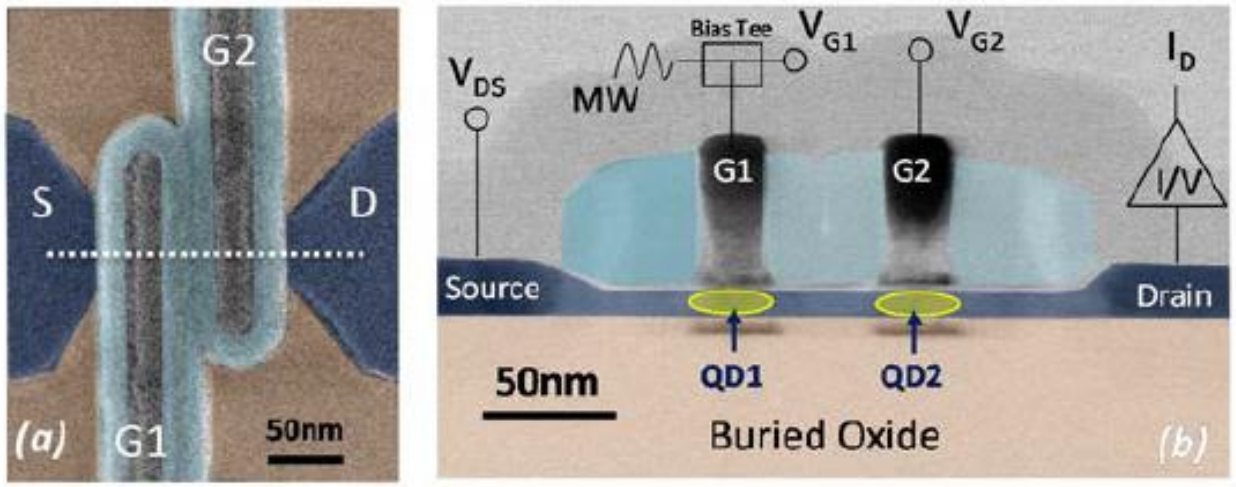
Implementation of semiconductor spin qubits



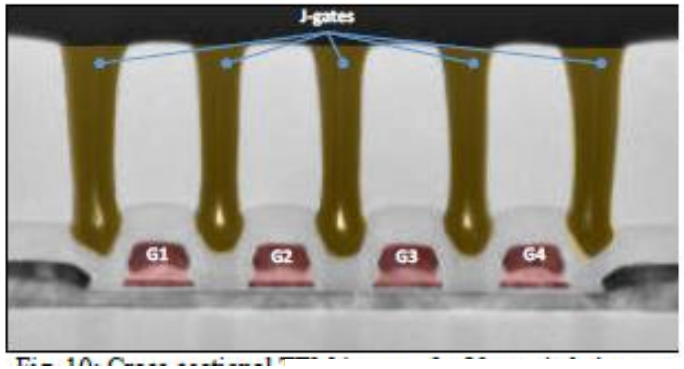
G. Burkhard et al. Rev.Mod.Physics. 95, 025003 (2023).

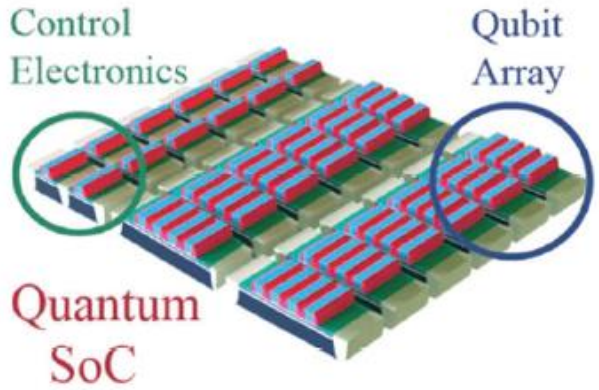
Qubits in fully-depleted silicon-on-insulator (FDSOI) technology

- spin degree of freedom of gate-confined holes in p-type devices
- In the case of holes, their inherently strong **spin-orbit coupling** offers the opportunity to perform single-qubit operations simply by a time-controlled microwave modulation of a gate voltage



S. De Franceschi et al SOI technology for quantum information processing *2016 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2016, pp. 13.4.1-13.4.4, doi: 10.1109/IEDM.2016.7838409.





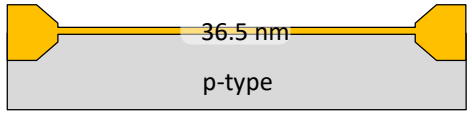
B. C. Paz et al., "FDSOI Platform for Quantum Computing," 2024 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2024, pp. 1-4, https://doi.org/10.1109/IEDM50854.2024.10873521

IMB-CNM quantum semiconductor device platform

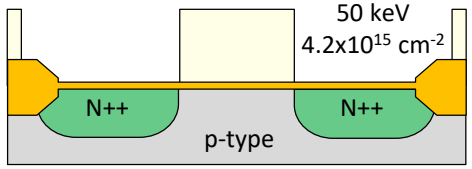
- **CSIC** semiconducting qubit module development on their internal 150mm process lines

  Development for test vehicle concluded. Low temperature characterization on-going

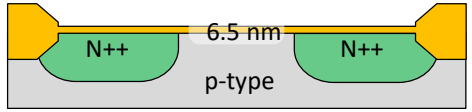
***(i)* 200 nm SiO2 as field oxide**



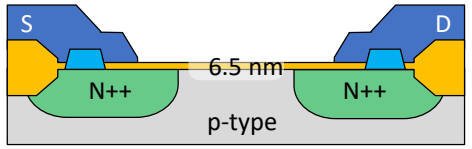
***(ii)* S/D implantation**



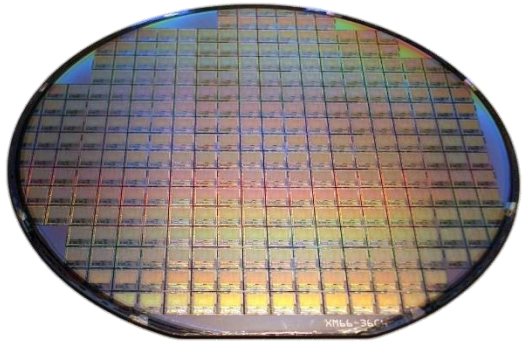
***(iii)* Gate oxidation**

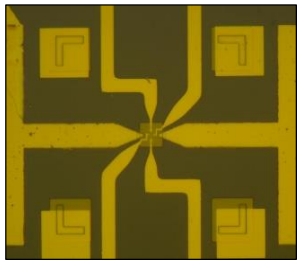


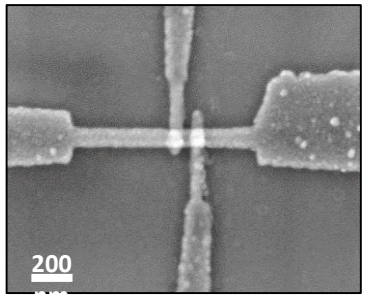
***(iv)* S/D contacts**

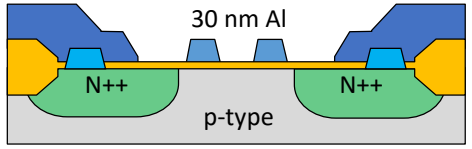


Si substrate | Photoresist
Silicon oxide | Contact windows
P/N well | S/D contacts

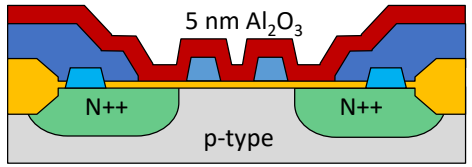




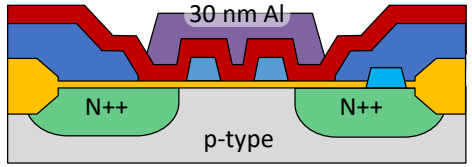




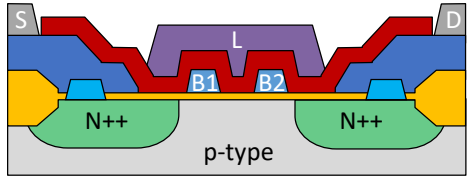
***(vi)* Dielectric layer**



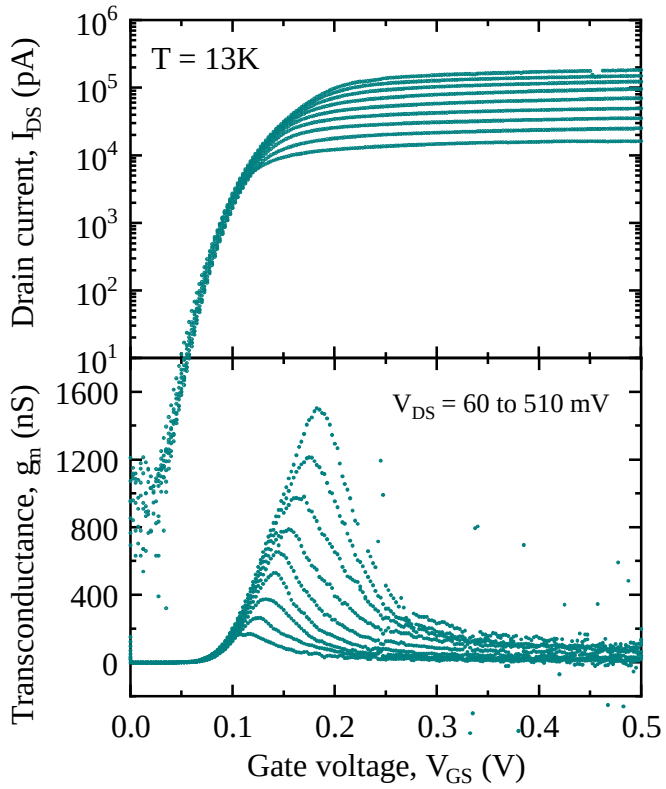
***(vii)* Lead gate**

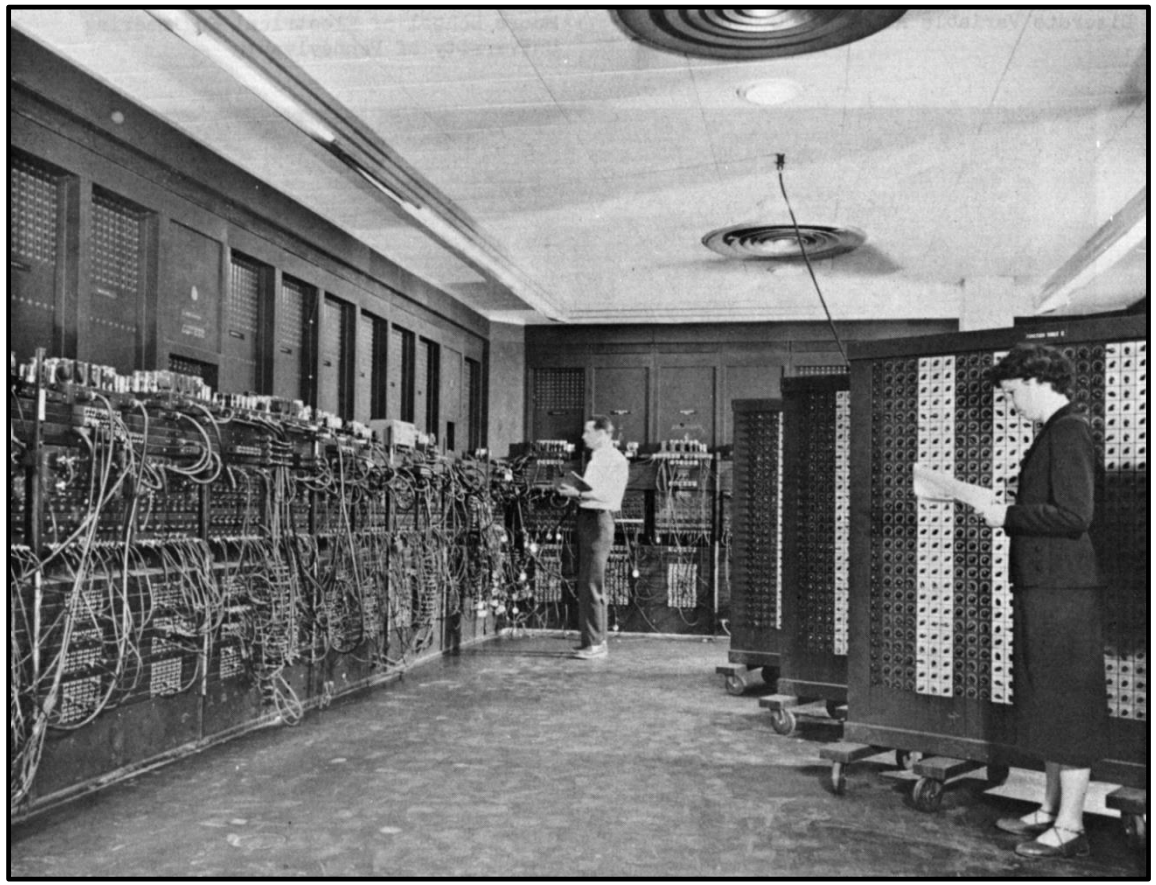


***(viii)* Metal contacts**



1st metal (Al) | Dielectric (Al_2O_3)
2nd metal (Al) | Metal contact (Al)





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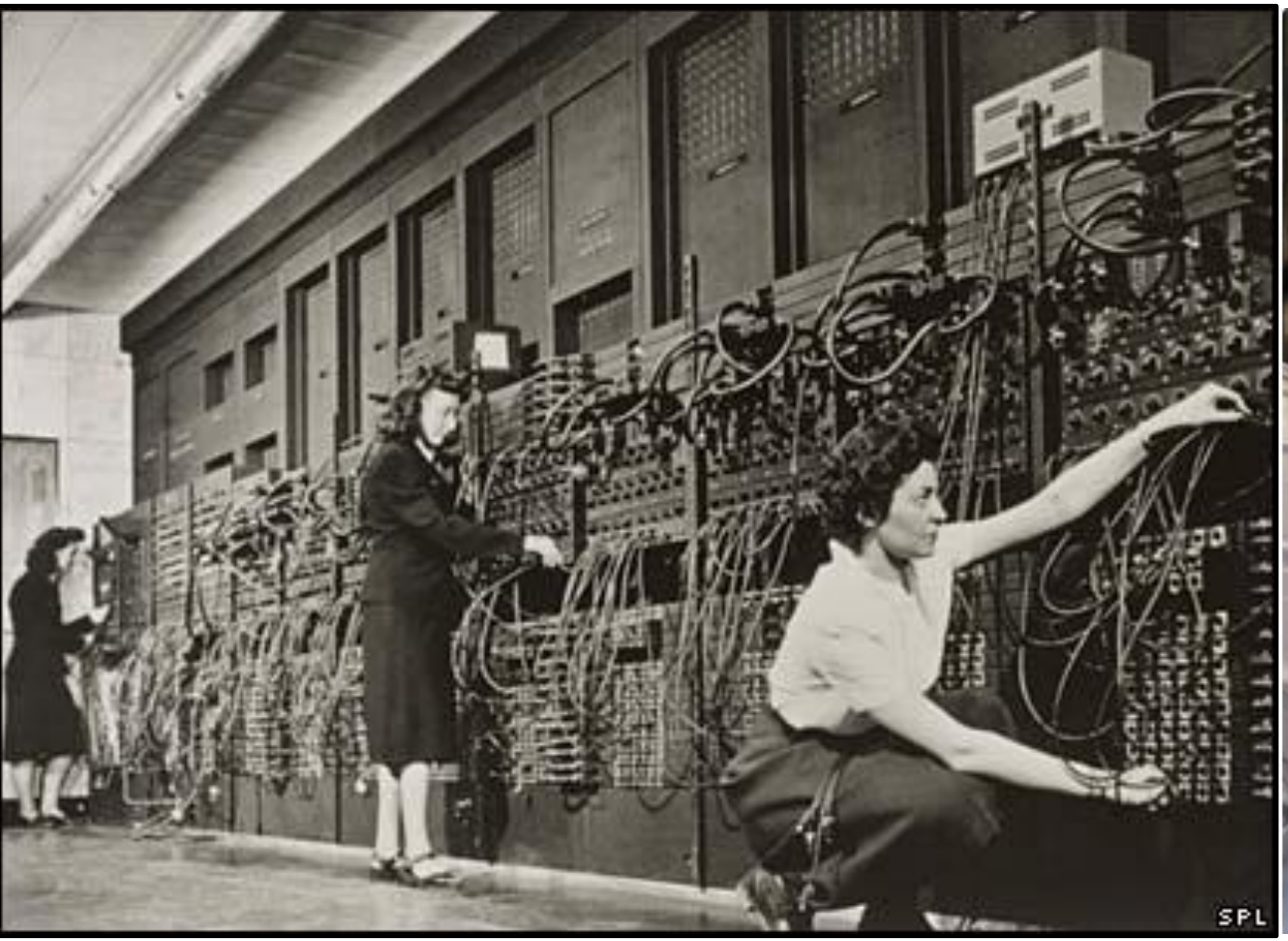

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